

# Matira5 Title Page/Index

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040	EMPTY	
041	CPU1 B2B connector	CPU1
042	EMPTY	
043	EMPTY	
044	EMPTY	

P.	Contents	Function
045	EMPTY	CPU1
046	EMPTY	
047	EMPTY	
048	EMPTY	
049	EMPTY	
050	EMPTY	N/A
051	EMPTY	
052	EMPTY	
053	EMPTY	
054	EMPTY	
055	EMPTY	
056	EMPTY	
057	EMPTY	
058	EMPTY	
059	EMPTY	
060	EMPTY	
061	EMPTY	
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076	PCH CLOCK/LAN/JTAG	
077	PCH USB/PCIE/SATA	
078	PCH DMI/PCIE UP/GPIO	
079	PCH GPIO	
080	PCH Power - 1OF2	
081	PCH Power - 2OF2	
082	PCH Ground	
083	STRAP	LOGIC
084	Miscellaneous	
085	EC Embedded Controller	EC
086	EC GPIO Expander	
087	CPLD - 1OF2	CPLD
088	CPLD - 2OF2	

P.	Contents	Function
089	GBE I219 Jacksonville	LAN
090	EMPTY	
091	EMPTY	
092	Audio Codec	AUDIO
093	Audio Connector	
094	USB 3.0 Connector - 1OF2	USB
095	USB 3.0 Connector - 2OF2	
096	INT USB 3.0 - 1OF2	
097	INT USB 3.0 - 2OF2	
098	Front Panel USB 3.0	
099	USB 3.1 TypeC - 1OF3	
100	USB 3.1 TypeC - 2OF3	
101	USB 3.1 TypeC - 3OF3	
102	SATA Connector	STORAGE
103	PS/2 KBMS/Serial	PS/2
104	Power Conn/Front Panel	CONN
105	Thermal Sensor	SENSOR
106	Fan Connector	FAN
107	TPM/SPI	TPM/SPI
108	Debug/Label/Misc	XDP
109	MERGED XDP - DCI	DCI
110	SMBUS MUX	SMBUS
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112	VR, CPU0 CORE CONTROLLER	CPU0 VR
113	VR, CPU0 CORE OUTPUT	
114	VR, CPU0_VCCSA OUTPUT	
115	VR, CPU0_VCCIO CONTROLLER	
116	VR, CPU0_VCCIO_PHASE	
117	VR, CPU0_VMCP PWM	
118	VR, CPU0_VMCP_PHASE	
119	VR, CPU0_1V0	CPU1 VR
120	VR, CPU1 CORE CONTROLLER	
121	VR, CPU1 CORE OUTPUT	
122	VR, CPU1_VCCSA OUTPUT	
123	VR, CPU1_VCCIO CONTROLLER	
124	VR, CPU1_VCCIO_PHASE	
125	VR, CPU1_VMCP PWM	
126	VR, CPU1_VMCP_PHASE	
127	VR, CPU1_1V0	CPU0 MEM VR
128	VR, CPU0_VDDQ012_PWM	
129	VR, CPU0_VDDQ012_OUT	
130	VR, CPU0_VDDQ345_PWM	
131	VR, CPU0_VDDQ345_OUT	
132	VR, CPU1_VDDQ012_PWM	

P.	Contents	Function
133	VR, CPU1_VDDQ012_OUT	CPU1 MEM VR
134	VR, CPU1_VDDQ345_PWM	
135	VR, CPU1_VDDQ345_OUT	
136	VR, MEMORY VTT	MEM VTT
137	VR, +PVNN	PCH VR
138	VR, +1V05/+1V8/ +GPPA_AUX	
139	VR, +5V/+3_3V	
140	VR, +5/+3.3V_STB& +3.3V_SLOT	SYS VR
141	LOADSWITCH, +5V/+3V	
142	VR, LOM2 2.5V & 2.1V	LOM VR
143	VR, LOM2 1.2V & 0.83V	
144	VR, VCC/VDD	USB3.1 VR
145	+P2V5_CPU0/1	CPU MEM VR
146	Changelist	

DC power page will updated  
once solution fixed

Title Page/Index  
Rev 0.1  
July/27/2015

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**TITLE** Title Page/Index

**DWG NO.** MATRISA 5

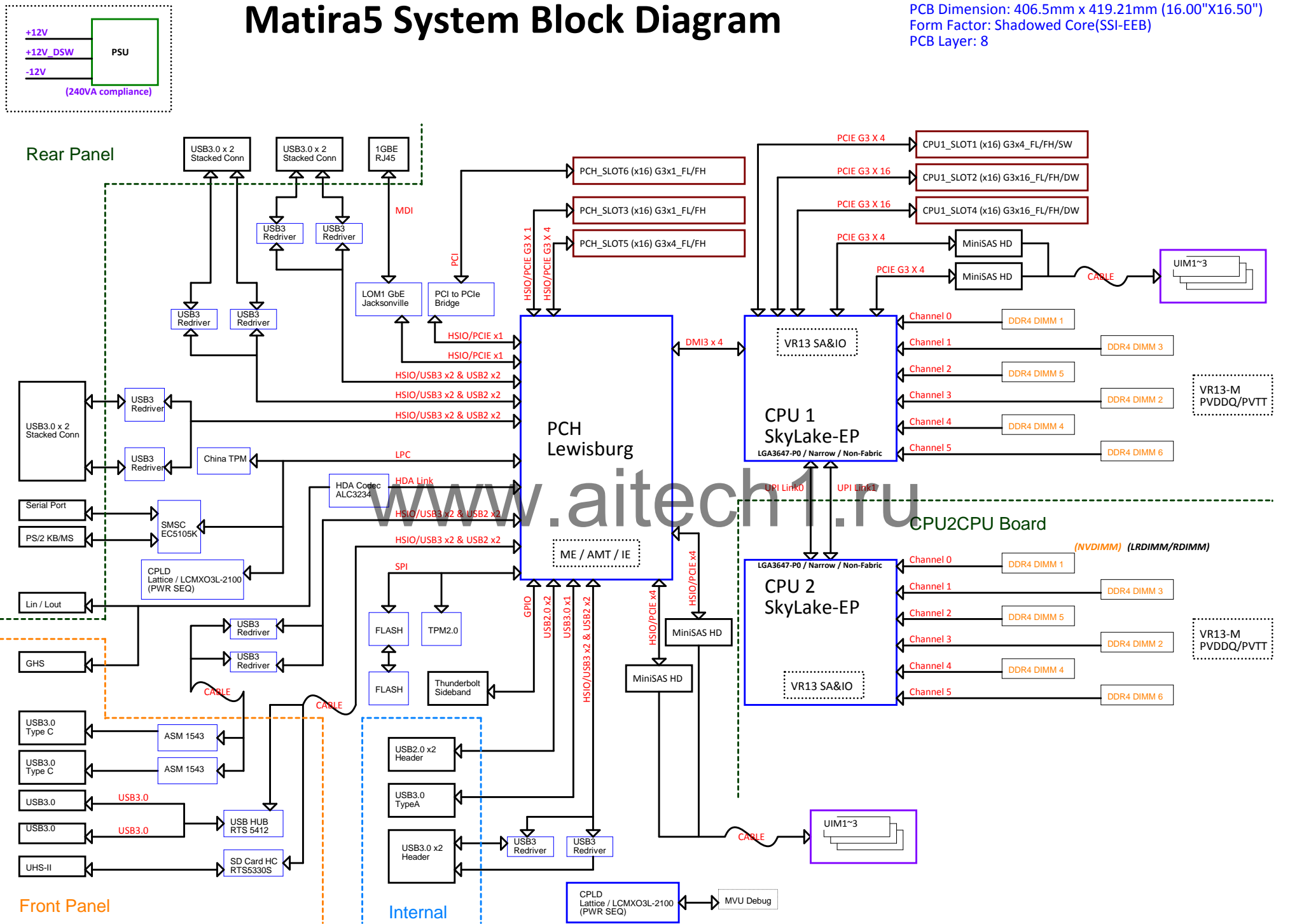
**REV.** X02

**DATE** Thursday, June 29, 2017

**SHEET** 1 of 150

# Matira5 System Block Diagram

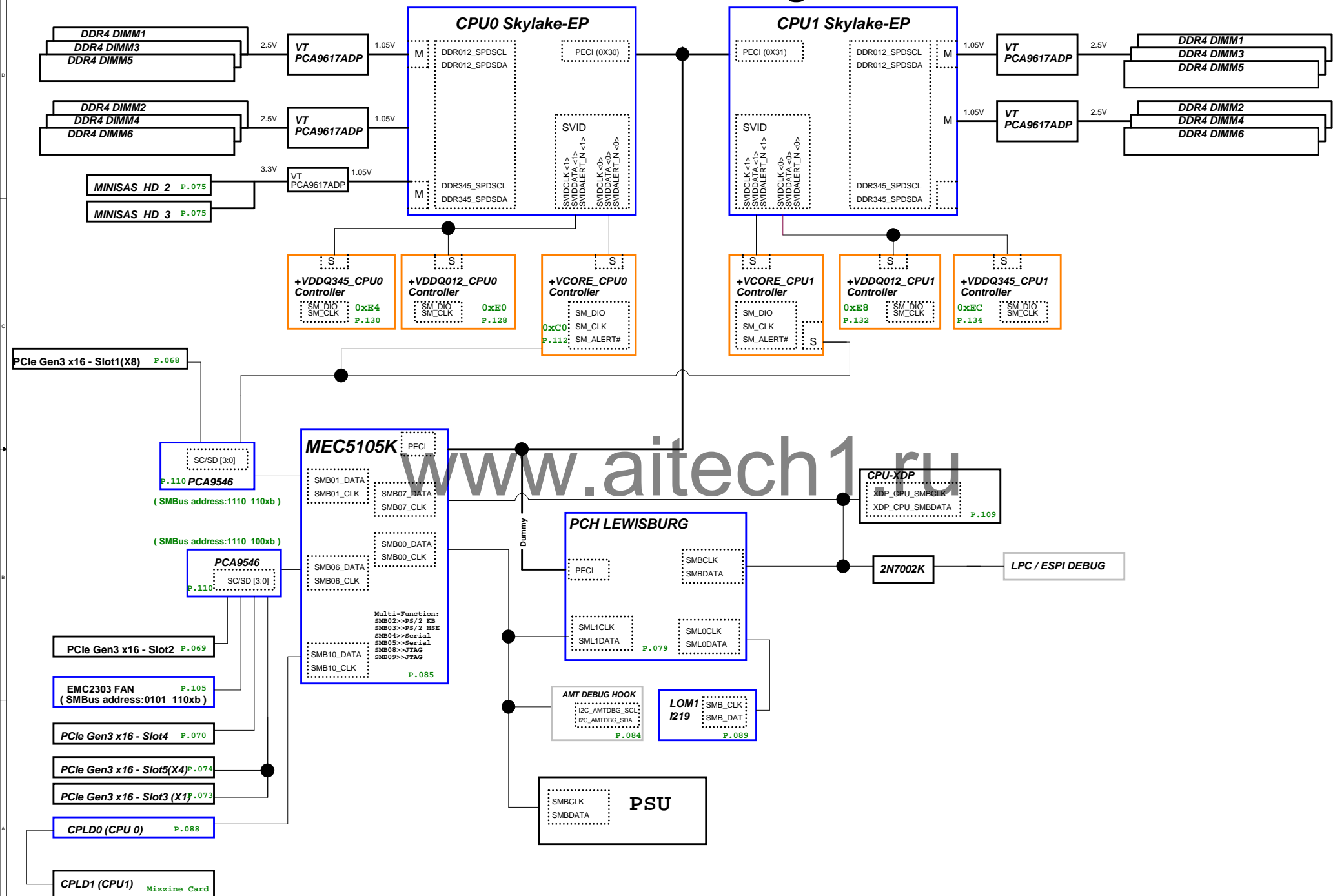
PCB Dimension: 406.5mm x 419.21mm (16.00"X16.50")  
Form Factor: Shadowed Core(SSI-EEB)  
PCB Layer: 8



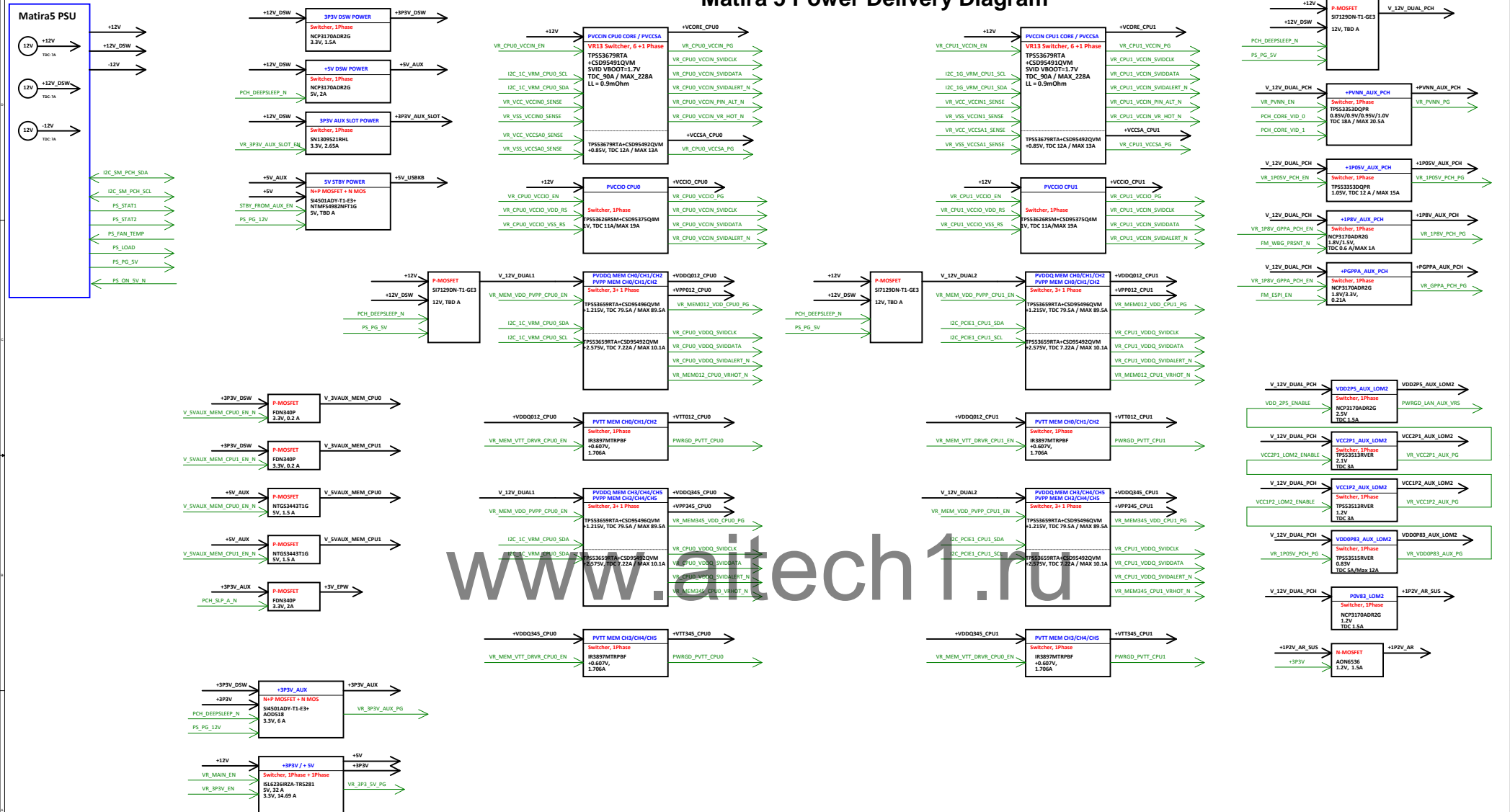
System Block Diagram  
Rev 0.2  
July/23/2015

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		<b>REV.</b> X02 <b>DATE</b> Thursday, June 29, 2017 <b>SHEET</b> 2 of 150	

## Matira 5 SMBUS & HWM Diagram



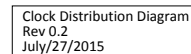
### Matira 5 Power Delivery Diagram



20150724 updat



## PCH is Clock Mode

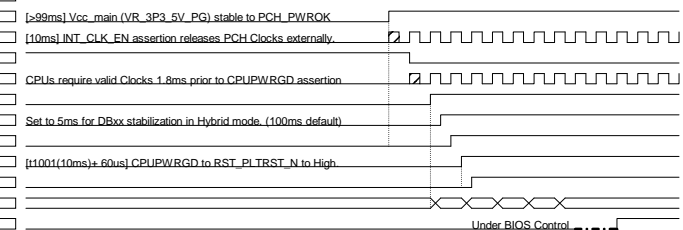


### G3 to S5 / S5 to S0 Timing Diagram

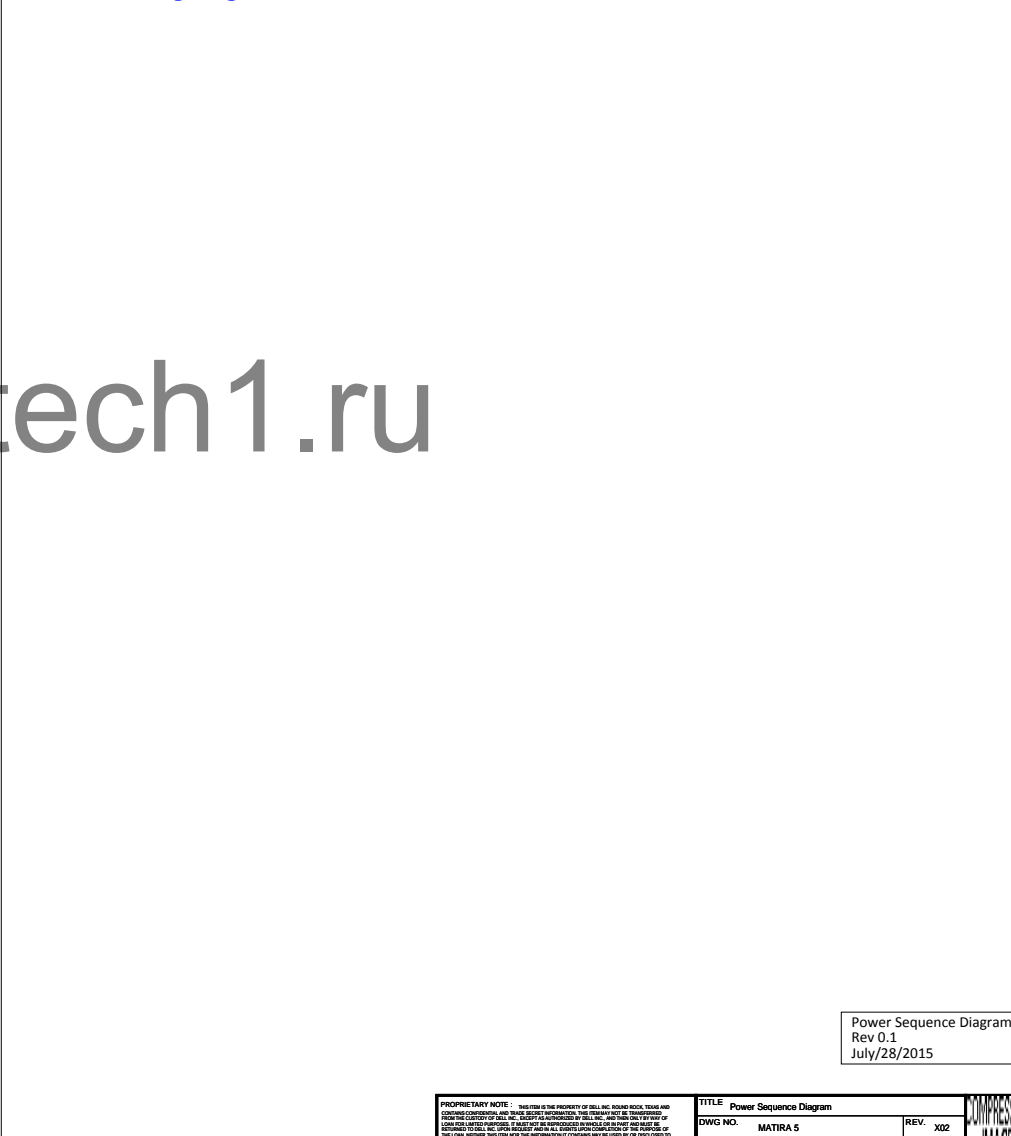
Board	PCH	V 3V VBAT
Board	PCH	PCH RTCRST_N
PSU	Board	+12V_DSW
Board	PCH	+5V_DSW / +3P3V_DSW
Board	PCH	VR_PCH_DSW_PWROK
Board	PCH	PCH_32M_RTCX21-N
PCH	CPUD / EC / VR	PCH_DEEPSLEEP_N
VR	VR	V 12V DUAL MemM
VR	ASMI142	+1P2V_AR_SUS
VR	Board	+3P3VAUX
CPUD / EC	VR	VR_3P3V_AUX_SLOT_EN
VR	Board	+3P3V_AUX_SLOT
CPUD / EC	VR	VR_1P8V_GPPA_PCH_EN
VR	Board	+1P8V_AUX_PCH (+GPPA_AUX_PCH)
CPUD / EC	VR	VR_P3VIN_EN
VR	Board	+P3VIN_AUX_PCH
CPUD / EC	VR	VR_1P05V_PCH_EN
VR	Board	+1P05V_AUX_PCH
VR	Board	VR_1P05V_PCH_PG
VR	LOM2	+VDDOPB3 AUX LOM2
VR	LOM2	+VOC1P2 AUX LOM2
VR	LOM2	+VCC2P1 AUX LOM2
VR	LOM2	+VDD2P5 AUX LOM2
EC5056	PCH	PCH_RSMRST_N
PCH	CPUD	CK 32K_SUSCLK
PCH	Board (CPUD / EC)	PCH_SUSWARM_N
Board	PCH	PCH_SUSACK_N
.....		
PCH	Board	PCH_WAKE_N
Board	PCH / CPUD / EC	PCH_PWRBRTN_N
PCH	Board / CPUD / EC	PCH_SLP_SIS_43-N
PCH	Board / CPUD / EC	PCH_SLP_A_N
VR	Board	+3V_EWP
PCH	VR	PCH_SLP_LAN_N
VR	LOM1	+3P3V_DSW_LAN
CPUD / EC	PSU	PS_ON
PSU	Board	+12V
PSU	Board (CPUD / EC)	PS_PG_12V (PS_PG_3P3_N)
CPUD / EC	Board	STRB_FROM_AUX_EN
VR	Board	+5V_USB8B
CPUD / EC	VR	VR_MAIN_EN (VR_3P3V_EN)
VR	Board	+5V
VR	Board	+3P3V
VR	Board	VR_3P3_5V_PG
VR	Board	+1P2V_AR
VR	PCH	+3P3VAUX
VR	PCH	+1P8V_AUX_PCH (+GPPA_AUX_PCH +P3VIN_AUX_PCH)
VR	PCH	+1P05V_AUX_PCH
VR	LOM2	+VDDOPB3 AUX LOM2
VR	LOM2	+VOC1P2 AUX LOM2
VR	LOM2	+VCC2P1 AUX LOM2
VR	LOM2	+VDD2P5 AUX LOM2
CPUD / EC	VR	VR_MEM_VDD_PVPP_CF
VR	DRAM / CPU	+VPP1(21345)_CPU1(0)
VR	DRAM / CPU	+VDD(012345)_CPU1(0)
VR	EC / CPUD	VR_MEM(0)_VDD_CPU1(0)
CPUD / EC	VR	VR_MEM_VTT_DRVVR_CPU1(0)
VR	DRAM	+VTT(012345)_CPU1(0)
CPUD / EC	Board	CPU_MEM_VDD_PG
Board	CPU	PWRGD_CPU1(0)_IMAI
CPUD / EC	VR	VR_CPU1(0)_VCCIO_EN
VR	CPU	+VCCIO_CPU1(0)
CPUD / EC	VR	VR_CPU1(0)_VCCIO_PG
CPUD / EC	VR	VR_CPU1(0)_VCCIN_EN
VR	CPU	+VCCORE_CPU1(0)
VR	CPUD / EC	VR_CPU1(0)_VCCIN_PG
VR	CPU	+VCCSA_CPU1(0)
VR	CPUD / EC	VR_CPU1(0)_VCCSA_PG



CPLD / EC	PCH	PCH_PWROK_PG
PCH	Board	PCH_isClocks
CPLD / EC	DB1x00Z	CLK_CPU_BCLKS_EN_N
DB1x00Z	Board	DB1x00Z_Clocks
PCH	CPLD / EC	PCH_PROC_PWRGD
CPLD / EC	CPU	PROC_PROC_PWRGD
CPLD / EC	PCH	PCH_SYS_PWROK
PCH	CPLD / EC	PCH_PLTRST_N
CPLD / EC	Board	PERST#
CFPU	CPLD / EC	H_CPU1x01_FVR_FAULT_GTL
CPU	DRAM	M_xxx_RESET_N



### S0 to S5 Timing Diagram



## Matira5 Rest / Power Good Map

***- To Be Updated -***  
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[illegible]

Matira 5 Strap/IRQ/IDSel Table

PCH Functional Strap

Signal	Usage	When Sampled	Comment
GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	<p>This Signal has a weak internal pull-down.</p> <p>This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.</p> <p><b>Bit 10 Boot BIOS Destination</b></p> <p>0 SPI 1 LPC/eSPI</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal pull-down is disabled after PLTRST# de-asserts.</li><li>If option 1 (LPC/eSPI) is selected, BIOS may still be placed on LPC/eSPI but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot.</li><li>Boot BIOS Destination Select to LPC by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® ME or LAN.</li></ol>
GPP_C5_SML0ALERT_IE#	eSPI_EN	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>0 = <b>LPC</b> functionality is selected.</p> <p>1 = <b>eSPI</b> functionality is selected.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal pull-down is disabled after RSMRST# de-asserts.</li></ol>
HDA_SDO	Flash Descriptor Security Override	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = <b>Enable</b> security measures defined in the Flash Descriptor.</p> <p>1 = <b>Disable</b> Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal pull-down is disabled after PLTRST# de-asserts.</li><li>Asserting HDA_SDO high on the rising edge of PWROK will also halt Intel Management Engine after Chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug.</li></ol>
GPP_H12_SML2ALERT_IE# /	Master or Slave Attached Flash	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>0 = Master attached Flash.</p> <p>1 = Slave Attached Flash.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal pull-down is disabled after RSMRST# de-asserts.</li></ol>
GPP_H15	ADR Timer Hold Off	RSMRST	<p>This signal has a weak internal pullup.</p> <p>0 = ADR Timer Hold off is enabled.</p> <p>1 = ADR Timer Hold off is not enabled.</p>
GPP_K9_LAN_NCST_ARB_OUT	LAN Aux Power	rising edge of Global Reset (find pin)	<p>This signal has a weak internal pull-down.</p> <p>0 = D3COLD is not supported.</p> <p>1 = Aux power is available and the 10GbE LAN should support the D3COLD power state if enabled to do so.</p>
SPI_MISO	SPI Buffer voltage	rising edge of RSMRST#	<p>If sampled low, then SPI Buffer is set to 1.8V. If high, then the buffer is 3.3V</p>
GPP_H18_SML4ALERT_N_IE_N	RSVD	rising edge of RSMRST#	<p>This pin has an internal pullup. This strap needs to be sampled high during the rising edge of RSMRST#</p>
GPP_K7	RSVD	rising edge of RSMRST#	<p>This pin has an internal pulldown. This strap needs to be sampled low during the rising edge of RSMRST#</p>
Signal	Usage	When Sampled	Comment
SPIO_MOSI	RSVD	rising edge of RSMRST#	<p>This pin has an internal pullup. This strap needs to be sampled high during the rising edge of RSMRST#</p>
GPP_B23_MEIE_SML1ALERT_N_PHOT_N	DCI Enable	rising edge of RSMRST#	<p>This pin has an internal pulldown. This strap needs to be sampled low during the rising edge of RSMRST#</p>
SPIO_IO_2	RSVD	rising edge of RSMRST#	<p>This pin has an internal pullup. This strap needs to be sampled high during the rising edge of RSMRST#</p>
SPIO_IO_3	RSVD	rising edge of RSMRST#	<p>This pin has an internal pullup. This strap needs to be sampled high during the rising edge of RSMRST#</p>

Signal	Usage	When Sampled	Comment
GPP_B14_SPKR	Top Swap Override	Rising edge of PCH_PWROK	<p>The signal has a weak internal pull-down.</p> <p>0 = <b>Disable</b> "Top Swap" mode. (Default)</p> <p>1 = <b>Enable</b> "Top Swap" mode. This inverts an address bit (defined in FITC) at the top of system BIOS space. This provides an alternate physical address that the processor accesses at boot.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal pull-down is disabled after PLTRST# de-asserts.</li><li>Software will not be able to clear the Top Swap bit until the system is rebooted.</li><li>The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCH, bit4).</li></ol>
GPP_B18	No Reboot	Rising edge of PCH_PWROK	<p>The signal has a weak internal pull-down.</p> <p>0 = <b>Disable</b> "No Reboot" mode.</p> <p>1 = <b>Enable</b> "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running Intel® ITP/XDP.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal pull-down is disabled after PLTRST# de-asserts.</li><li>The status of this strap is readable using the NO REBOOT bit (Chipset Configuration Registers: RCBA + Offset 3410h:Bit 5).</li></ol>
GPP_C2_SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>0 = <b>Disable</b> Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).</p> <p>1 = <b>Enable</b> Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AHT with TLS and Intel® Small Business Advantage (Intel® SBA) with TLS.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"><li>The internal pull-down is disabled after RSMRST# de-asserts.</li></ol>

PCH IRQ

Name	Type	Description
GPP_A6_SERIRQ_ESPI_CS1#	I/O	Serial Interrupt Request <b>Note:</b> An external pull-up is required
GPP_A7_PIRQA#_ESPI_ALERT0#	I/OD	PCI Interrupt Request A <b>Note:</b> Note: An external pull-up is required

CPU Functional Strap

Signal Name	Description
BIST_ENABLE	BIST Enable Strap. Input which allows the platform to enable or disable BIST self test (BIST) on the processor. This signal is pulled up on the die. Refer to Table 2-8 for details.
BMCINIT	BMC Initialization Strap. Indicates whether Service Processor Boot Mode should be used. Used in combination with FRMAGENT and SOCKET_ID inputs. 0: Service Processor Boot Mode Disabled. Example boot modes: Local PCH (this processor hosts a legacy PCH with firmware behind it) 1: Service Processor Boot Mode Enabled. In this mode of operation, the processor performs the absolute minimum internal configuration and then waits for the Service Processor to complete its initialization. The socket boots after receiving a "GO" handshake signal via a firmware scratchpad register. This signal is pulled down on the die, refer to Table 2-8 for details. For further details see <i>Skylake Server External Design Specification (EDS), Volume One: Architecture</i>
DMIMODE_OVERRIDE	BMCINIT, DMIMODE_OVERRIDE, FRMAGENT, and LEGACY_SKT, whether local or remote, whether the boot PCH is attached, whether the socket is legacy and whether port0 is DMI or PCIe.
SAFE_MODE_BOOT	Safe Mode Boot Strap. SAFE_MODE_BOOT allows the processor to wake up safely by disabling all clock gating. This allows BIOS to load registers or patches if required. This signal is sampled after PWRGOOD assertion. The signal is pulled down on the die. Refer to Table 2-8 for details.

FRMAGENT	Bootable Firmware Agent Strap. This input configuration strap used in combination with SOCKET_ID to determine whether the socket is a legacy socket, bootable firmware agent is present, and DMI links are used in PCIe* mode (instead of DMI3 mode). The firmware flash ROM is located behind the local PCH attached to the processor via the DMI3 interface. This signal is pulled down on the die, refer to Table 2-8 for details. For further details see <i>Skylake Server External Design Specification (EDS), Volume One: Architecture</i> .
PM_FAST_WAKE_N	Power Management Fast Wake. Enables quick package C3 - C6 exits of all sockets. Asserted if any socket detects a break from package C3 - C6 state requiring all sockets to exit the low power state to service a snoop, memory access, or interrupt. Expected to be wired-OR among all processor sockets within the platform.
PROC_ID [1:0]	This output can be used by the platform to determine if the installed processor is a Skylake Server, Cannonlake Server, or a future processor planned for Purley. There is no connection to the processor silicon for this signal. The processor package grounds or floats the pin to set '0' or '1', respectively. 00: Skylake Server 01: Cannonlake 10: Reserved 11: Reserved.
SOCKET_ID[2:0]	SOCKET_IDStrap. Socket identification configuration straps for establishing the PECI address and Intel UPI Node ID. This signal is used in combination with FRMAGENT to determine whether the socket is a legacy socket, bootable firmware agent is present, and DMI links are used in PCIe* mode (instead of DMI3 mode). Each processor socket consumes one Node ID, and there are 128 Home Agent tracker entries. This signal is pulled down on the die. Refer to Table 2-8 for details. For further details see <i>Skylake Server External Design Specification (EDS), Volume One: Architecture</i> SOCKET_ID[1:0] is used for 25 platforms and SOCKET_ID[2:0] is implemented on 45/85 platforms. This is an asynchronous signal to other clocks in the processor. Refer to the Platform Design Guide for details.
TXT_AGENT	Intel® Trusted Execution Technology (Intel® TXT) Agent Strap. 0 = Default. The socket is not the Intel TXT Agent. 1 = The socket is the Intel TXT Agent. The legacy socket (identified by SOCKET_ID[1:0] = 00b) with Intel TXT Agent should always set the TXT_AGENT to 1b. This signal is pulled down on the die, refer to Table 2-8 for details. For further details see <i>Skylake Server External Design Specification (EDS), Volume One: Architecture</i>
TXT_PLTEN	Intel Trusted Execution Technology (Intel TXT) Platform Enable Strap. 0 = The platform is not Intel TXT enabled. All sockets should be set to zero. Scalable DP (sDP) platforms should choose this setting if the Node Controller does not support Intel TXT. 1 = Default. The platform is Intel TXT enabled. All sockets should be set to one. In a non-Scalable DP platform this is the default. When this is set, Intel TXT functionality requires user to explicitly enable Intel TXT via BIOS setup. This signal is pulled up on the die, refer to Table 2-8 for details. For further details see <i>Skylake Server External Design Specification (EDS), Volume One: Architecture</i>
LEGACY_SKT	BMCINIT, FRMAGENT, LEGACY_SKT together determine the boot mode (SSP, Intel UPI Link boot modes, DCF boot), whether local or remote, whether the boot PCH is attached, whether the socket is legacy and whether port0 is DMI or PCIe (Gen1/2. With one exception, this input configuration strap indicates to the processor that it is the legacy socket. The legacy SKT must be strapped for NODE ID 0, via the SKIT ID pins. There is only 1 legacy SKT in a partition.
PKGID[2:0]	An indicator to the Purley platform of the Intel OmniPath configuration.
SOCKET_ID2	Asynchronous to other clocks in the processor.

## Matira 5 GPIO Table (1 of 2)

**-To Be Updated-**

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**MEC5055 (Cont.)**  
**ECE5048**

## Matira 5 GPIO Table (1 of 2)

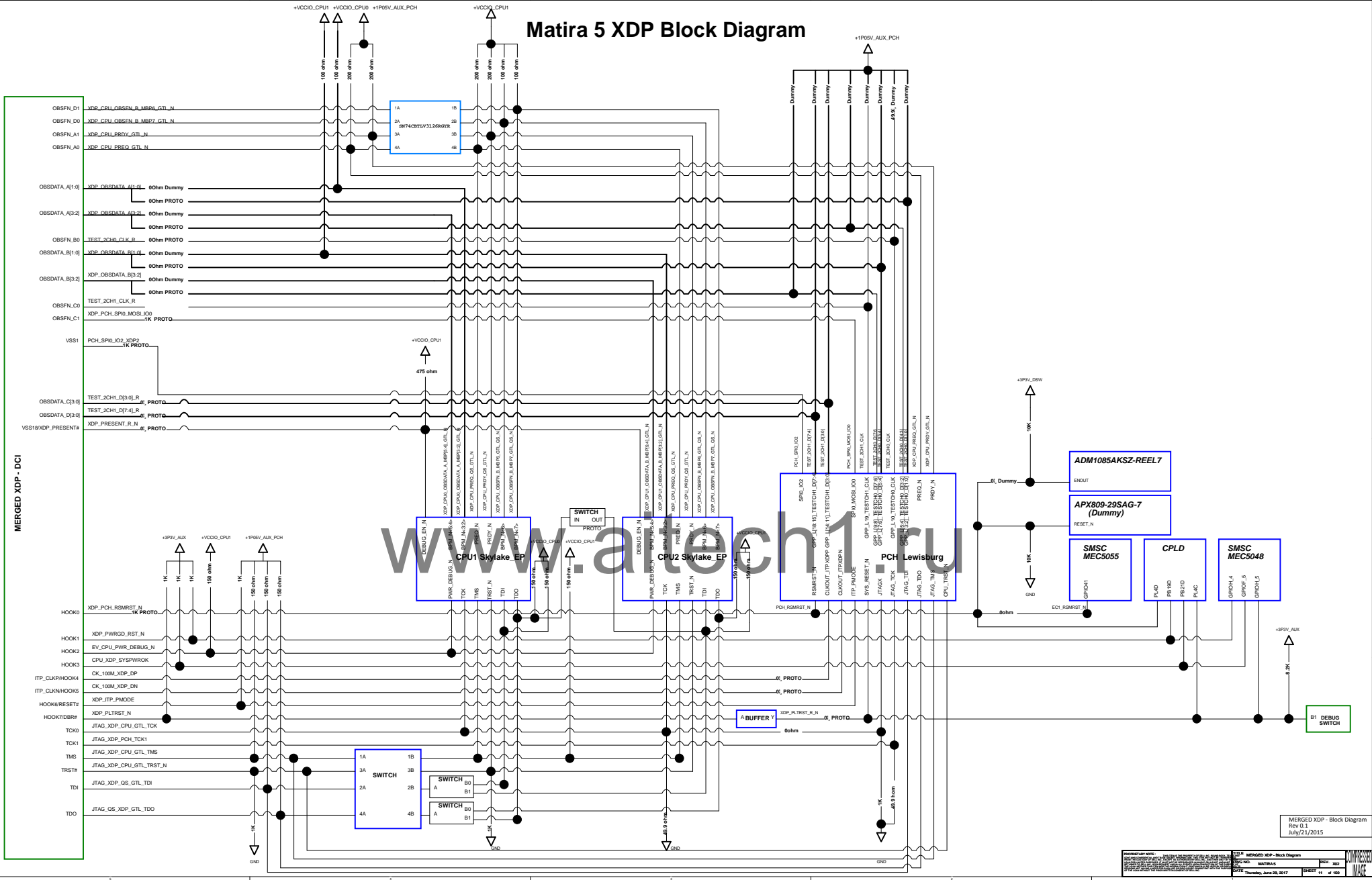
GPIO Table (2 of 2)  
Rev 0.5  
Feb/24/2014

**-To Be Updated-**

[illegible]

# Matira 5 XDP Block Diagram

MERGED XDP - DCI

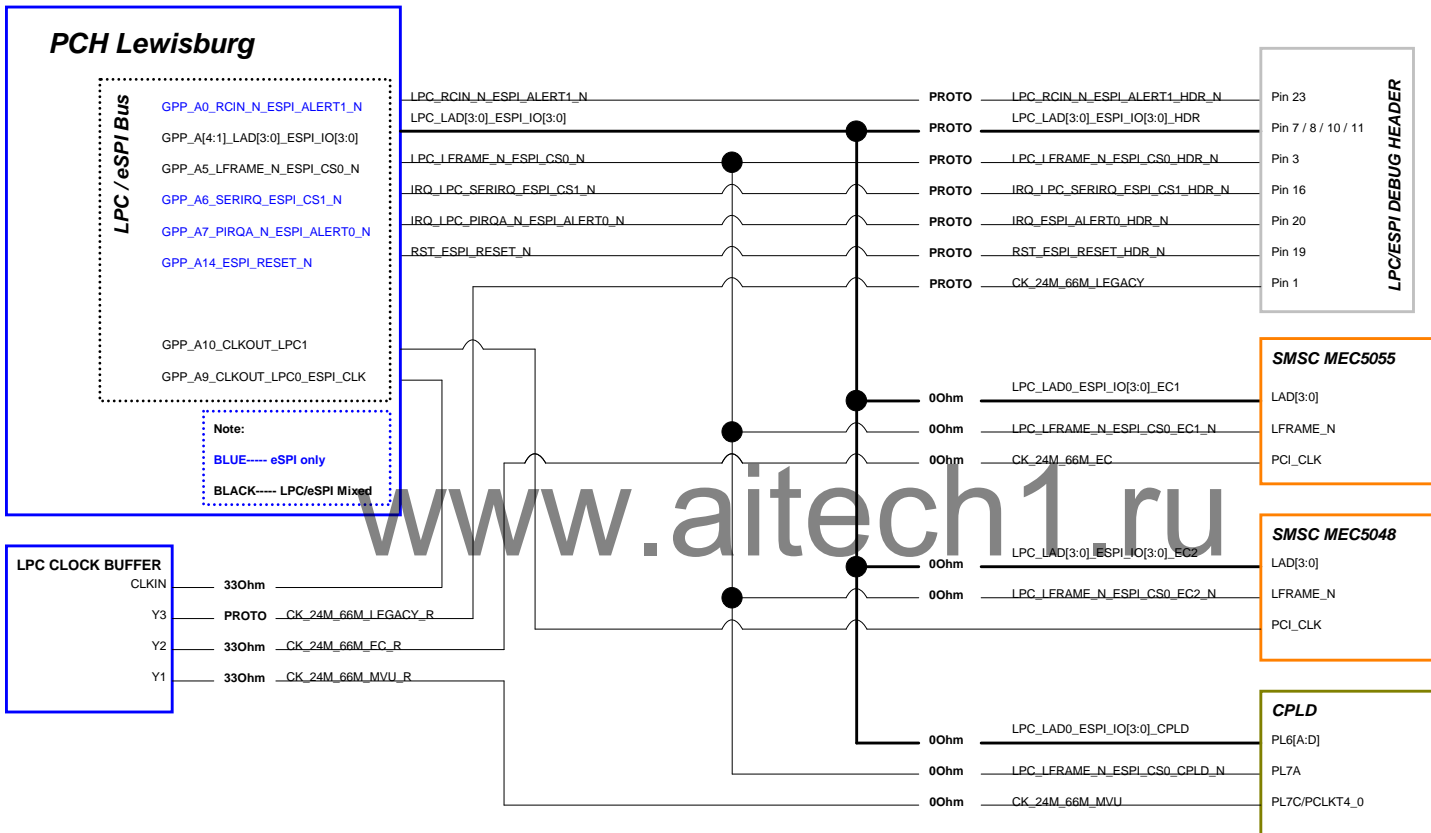


MERGED XDP - Block Diagram  
Rev 0.1  
July 23/2015

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# Matira 5 LPC/eSPI Block Diagram



LPC/eSPI Block Diagram  
Rev 0.2  
July/27/2015

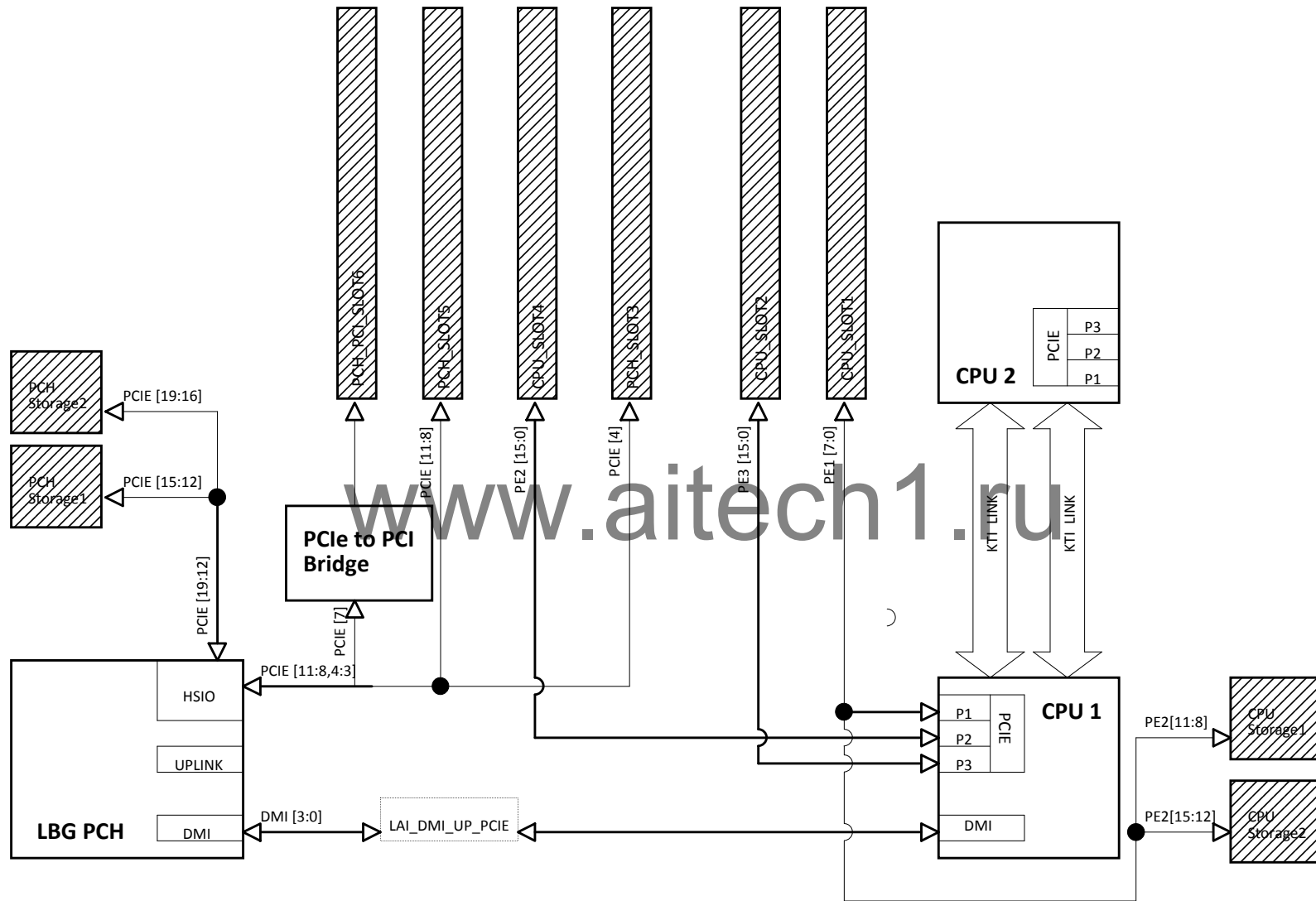
**- To Be Updated -**  
**www.aitech1.ru**

# Matira 5 System Power Rail

No.	Power Rails	Voltage	S0	M3		Moff	DSW	G3	Source	Control Signal
				S3	S4/S5					
1	V_3V_VBAT	3V	ON	ON	ON	ON	ON	ON	RTC Battery	RTC Battery
2	+12V_DSW	12V	ON	ON	ON	ON	ON	OFF	PSU	Adaptor in
3	+5V_DSW	5V	ON	ON	ON	ON	ON	OFF	+12V_DSW	Adaptor in
4	+3P3V_DSW	3.3V	ON	ON	ON	ON	ON	OFF	+12V_DSW	Adaptor in
5	V_12V_DUAL1/2_MEM1/2	12V	ON	ON	ON	ON	ON	OFF	+12V/+12V_DSW	PCH_DEEPSLEEP_N/PS_PG_5V
6	+3P3V_AUX	3.3V	ON	ON	ON	ON	OFF	OFF	+3P3V/+3P3V_DSW	PCH_DEEPSLEEP_N/PS_PG_12V
7	+5V_AUX	5V	ON	ON	ON	ON	OFF	OFF	+5V_DSW	PCH:PCH_DEEPSLEEP_N
8	V_12V_DUAL_PCH	12V	ON	ON	ON	ON	OFF	OFF	+12V/+12V_DSW	PCH_DEEPSLEEP_N/PS_PG_5V
9	+1P8V_AUX_PCH	1.8V	ON	ON	ON	ON	OFF	OFF	V_12V_DUAL_PCH	CPLD (EC5055): VR_1P8V_GPPA_PCH_EN
10	+PGPPA_AUX_PCH	3.3V/1.8V	ON	ON	ON	ON	OFF	OFF	V_12V_DUAL_PCH	CPLD (EC5055): VR_1P8V_GPPA_PCH_EN
11	+PVNN_AUX_PCH	1V	ON	ON	ON	ON	OFF	OFF	V_12V_DUAL_PCH	CPLD(EC5048):VR_PVNN_EN
12	+1P05V_AUX_PCH	1.05V	ON	ON	ON	ON	OFF	OFF	V_12V_DUAL_PCH	CPLD(EC5055): VR_1P05V_PCH_EN
13	+3P3V_AUX_SLOT	3.3V	ON	ON	ON	ON	OFF	OFF	+12V_DSW	CPLD(EC5055): VR_3P3AUX_SLOT_EN
14	+VDD2P5_AUX_LOM2	2.5V	ON	ON	ON	ON	OFF	OFF	V_12V_DUAL_PCH	VR_VCC2P1_AUX_PG
15	+VCC2P1_AUX_LOM2	2.1V	ON	ON	ON	ON	OFF	OFF	V_12V_DUAL_PCH	VR_VCC1P2_AUX_PG
16	+VCC1P2_AUX_LOM2	1.2V	ON	ON	ON	ON	OFF	OFF	V_12V_DUAL_PCH	VR_VDD0P83_AUX_PG
17	+VDD0P83_AUX_LOM2	0.83V	ON	ON	ON	ON	OFF	OFF	V_12V_DUAL_PCH	VR_1P05V_PCH_PG
18	+1P2V_AR_SUS	1.2V	ON	ON	ON	ON	OFF	OFF	V_12V_DUAL_PCH	V_12V_DUAL_PCH
19	+3V_EPW	3.3V	ON	ON	ON	OFF	OFF	OFF	+3P3V_AUX	PCH:PCH_SLP_A_N
20	+3P3V_DSW_LAN	3.3V	ON	ON	ON	ON	OFF	OFF	+3P3V_DSW	PCH:PCH_SLP_LAN_N
21	V_3VAUX_MEM_CPU0/1	3.3V	ON	ON	ON	ON	OFF	OFF	+3P3V_DSW	CPLD(EC5055): V_5VAUX_MEM_CPU0/1_EN_N
22	V_5VAUX_MEM_CPU0/1	5V	ON	ON	ON	ON	OFF	OFF	+5V_DSW	CPLD(EC5055): V_5VAUX_MEM_CPU0/1_EN_N
23	+5V_USBKB	5V	ON	ON	OFF	OFF	OFF	OFF	+5V/+5V_DSW	CPLD(EC5055): STBY_FROM_AUX_EN & PS_PG_12V
24	+VDDQ012/345_CPU0/1	1.2V	ON	ON	OFF	OFF	OFF	OFF	V_12V_DUAL1/2_MEM1/2	CPLD (EC5055) : VR_MEM_VDD_PVPP_CPU[1:0]_EN
25	+VPP012/345_CPU0/1	2.6V	ON	OFF	OFF	OFF	OFF	OFF	V_12V_DUAL1/2_MEM1/2	CPLD (EC5055) : VR_MEM_VDD_PVPP_CPU[1:0]_EN
26	+VTT012/345_CPU0/1	1.2V	ON	OFF	OFF	OFF	OFF	OFF	+VDDQ012/345_CPU0/1	MEM_VTT_DRVR_CPU0/1_EN
27	+12V	12V	ON	OFF	OFF	OFF	OFF	OFF	PSU	PS_ON
28	+VCORE_CPU0/1	1.8V	ON	OFF	OFF	OFF	OFF	OFF	+12V	CPLD (EC5055) : VR_CPU[1:0]_VCCIN_EN
29	+VCCSA_CPU0/1	1.8V	ON	OFF	OFF	OFF	OFF	OFF	+12V	CPLD (EC5055) : VR_CPU[1:0]_VCCIN_EN
30	+VCCIO_CPU0/1	1V	ON	OFF	OFF	OFF	OFF	OFF	+12V	CPLD (EC5055) : VR_CPU0/1_VCCIO_EN
31	+5V	5V	ON	OFF	OFF	OFF	OFF	OFF	+12V	CPLD (EC5055) : VR_MAIN_EN
32	+3P3V	3.3V	ON	OFF	OFF	OFF	OFF	OFF	+12V	CPLD (EC5048) :VR_3P3V_EN
33	+P2V5_CPU0/1	2.5V	ON	OFF	OFF	OFF	OFF	OFF	+VPP012_CPU0/1	CPLD (EC5055) : FM_SLPS3_P2V5_CPU0[1:0]_N
34	+1P2V_AR	1.2V	ON	OFF	OFF	OFF	OFF	OFF	+1P2V_AR_SUS	Power_+3P3V
35	+1P5V_AVDD	1.5V	ON	OFF	OFF	OFF	OFF	OFF	+3P3V	Power_+3P3V
36	-12V	-12V	ON	OFF	OFF	OFF	OFF	OFF	PSU	PS_ON

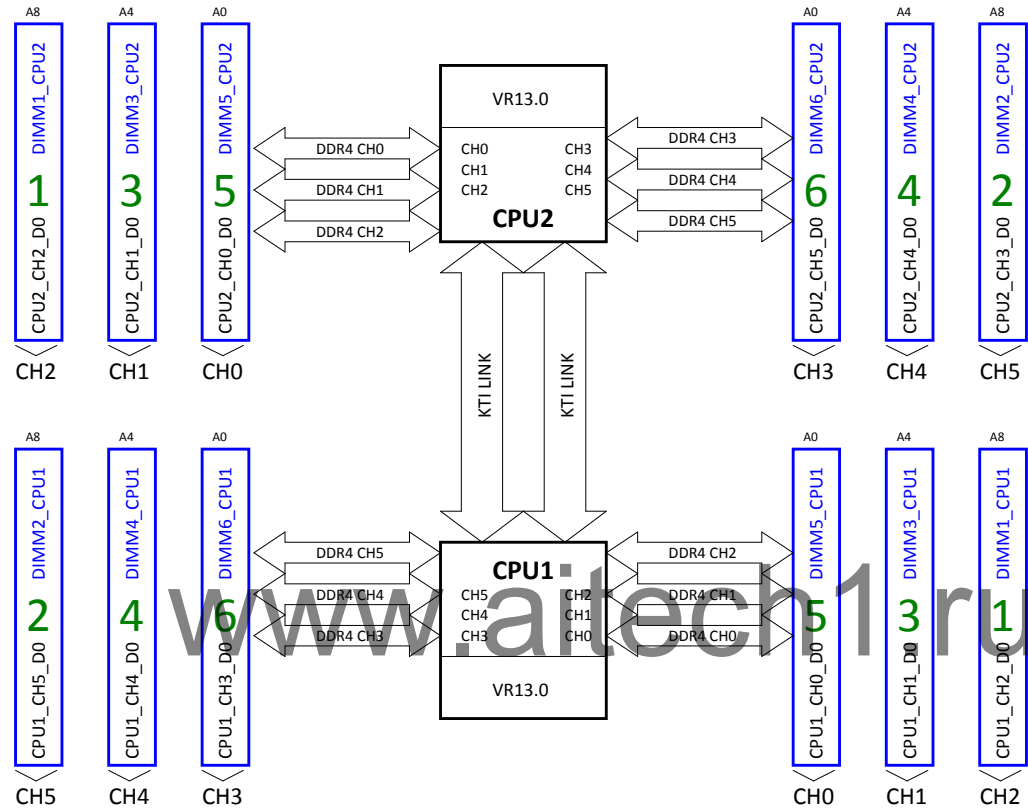
System Power Rail  
Rev 0.2  
July/27/2015

# Matira 5 PCIe Connection Diagram



PCIe Connection Diagram  
Rev 0.2  
July/23/2015

# Matira 5 Memory Connection Diagram



SILKSCREEN	CHANNEL	DIMM	SA[2:0]	SPD	TSOD
DIMM1 DIMM7	0	0 1	000 001	0xA0 0xA2	0x30 0x32
DIMM3	1	0	010	0xA4	0x34
DIMM5	2	0	101	0xA8	0x38
DIMM2 DIMM8	3	0 1	000 001	0xA0 0xA2	0x30 0x32
DIMM4	4	0	010	0xA4	0x34
DIMM6	5	0	101	0xA8	0x38

Memory Connection Diagram  
Rev 0.3  
11/12/2014

**- To Be Updated -**  
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# Matira5 PCB Stackup

## Foxconn stackup design

Layer NO.	Layer Name	Min. layer thickness (mil)	Typical layer thickness (mil)	Max. layer thickness (mil)	Dielectric Constant	Remark
	Solder Mask	0.40	0.50	1.80	3.70	
L1	Signal	1.40	1.90	2.40	NA	1.5 oz [with. Plating]
	Prepreg	2.20	2.70	3.30	3.90	
L2	Power/Gnd	1.00	1.20	1.40	NA	1 oz
	Core	3.50	4.00	4.50	3.90	
L3	Signal	1.00	1.20	1.40	NA	1 oz
	Prepreg	NA	15.00	NA	3.90	
L4	Power/Gnd	2.20	2.40	2.60	NA	2 oz
	Core	4.00	4.00	6.00	3.90	
L5	Power/Gnd	2.20	2.40	2.60	NA	2 oz
	Prepreg	NA	15.00	NA	3.90	
L6	Signal	1.00	1.20	1.40	NA	1 oz
	Core	3.50	4.00	4.50	3.90	
L7	Power/Gnd	1.00	1.20	1.40	NA	1 oz
	Prepreg	2.20	2.70	3.20	3.90	
L8	Signal	1.40	1.90	2.40	NA	1.5 oz [with. Plating]
	Solder Mask	0.40	0.50	1.80	3.70	
Total thickness			61.80			

Solder Mask	Min.	Typical	Max.
Solder Mask (a)	0.4 mil	0.7 mil	2.4 mil
Solder Mask (b, d)	0.4 mil		
Solder Mask (c)	0.4 mil	0.5 mil	1.8 mil

Notes :

\*2: Spacing of plane 4 to plane 5 must be 4 to 6 mils

\*3: Spacing of layer 3 to plane 4 must be at least 3x the distance of plane 2 to layer 3 (similarly w/ layer 6 and planes 5 & 7)

\*4: Thickness spec.: 63 +/-6 mils

**PCB Thickness :** 63 mils

**PCB Thickness Tolerance :** +/- 6 mils

## Impedance Calculation

Outer layer				Inner layer			
SPEC		Our design		SPEC		Our design	
Impedance target	Signal Type	Trace width/ Spacing (mil)	Simulation impedance(Ω)	Impedance target	Signal Type	Trace width/ Spacing (mil)	Simulation impedance(Ω)
50	Single-ended	4	51.33	50	Single-ended	5	49.9
±10%	Single-ended	6.5	40.25	±10%	Single-ended	8	39.56
±10%	Differential	5/7/5	85.17	±10%	Differential	5.3/6.2/5.3	85.3
±10%	Differential	4.5/13.5/4.5	94.42	±10%	Differential	5.1/10.3/5.1	93.32
±10% ; ±10% (Diff.)	Differential	4.01/13.99/4.01	99.76 (Diff.) 51.27 (Single-ended)	±10% ; ±10% (Diff.)	Differential	4.6/13/4.6	99.79 (Diff.) 51.76 (Single-ended)
±10% ; ±10% (Single-ended)				±10% ; ±10% (Single-ended)			

PCB Stackup  
Rev 0.1  
May/20/2015

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TITLE PCB Stackup  
DWG NO. MATIRA 5  
DATE Thursday, June 29, 2017  
REV. X02  
SHEET 18 of 150

COMPRESSED  
IMAGE





TITLE CPU0 Misc		COMPRESSED IMAGE
DWG NO. MATIRA 5	REV. X02	
DATE Thursday, June 29, 2017	SHEET 19 of 150	

Skylake\_E  
NOROMSkylake\_  
NOBOM

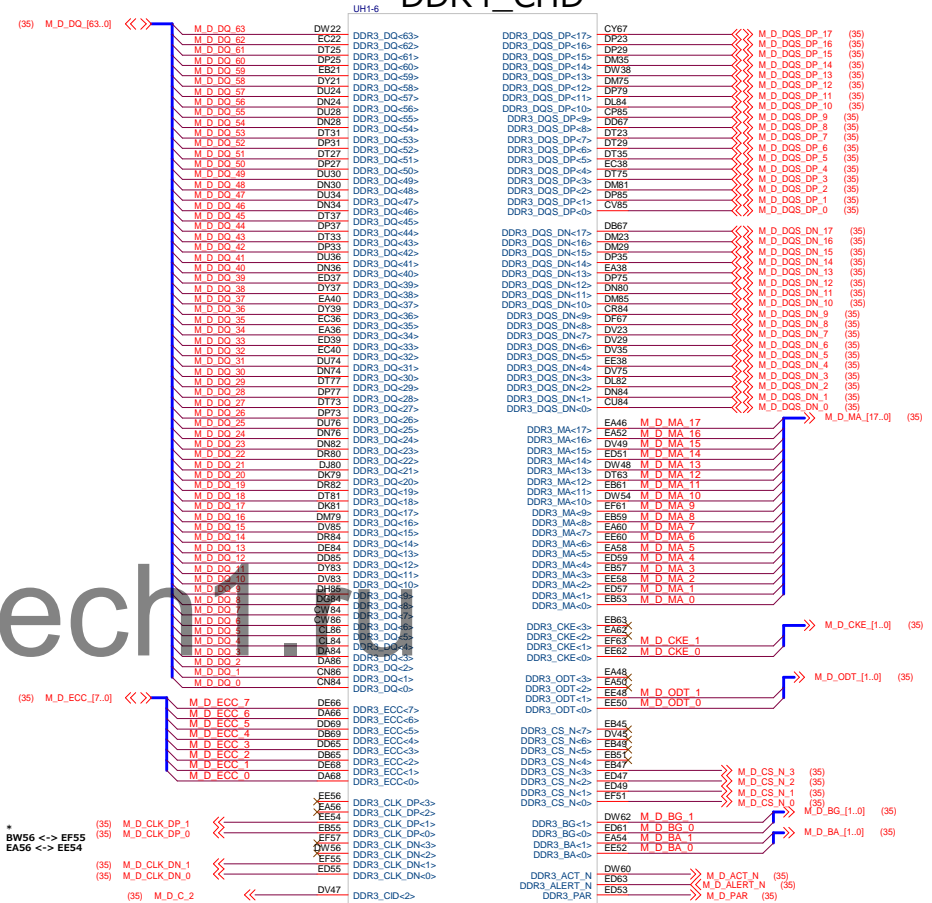
TITLE CPU0 DDR4 CHA/CHB		
DWG NO. MATIRA 5		REV. X02
DATE Thursday, June 29, 2017	SHEET 20 of 150	

COMPRESSED  
IMAGE

## DDR4\_CHC



## DDR4\_CHD



## DDR4\_CHE

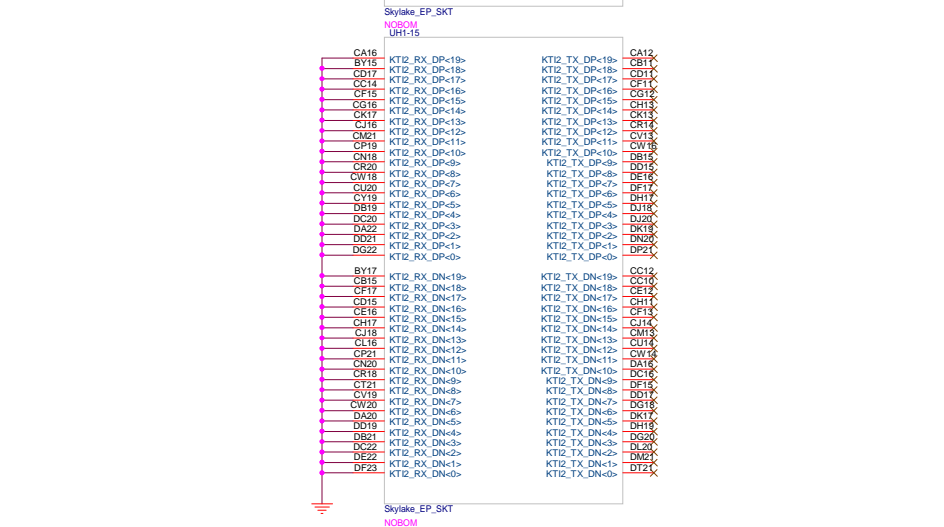
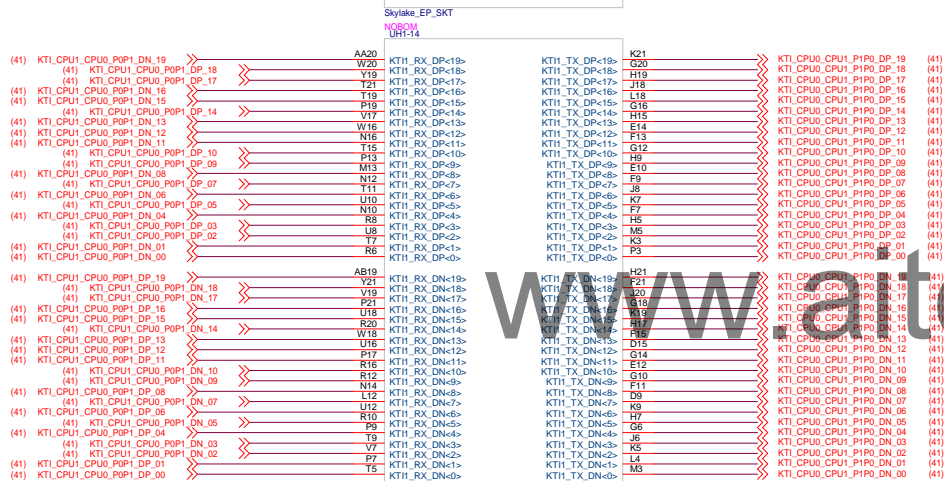
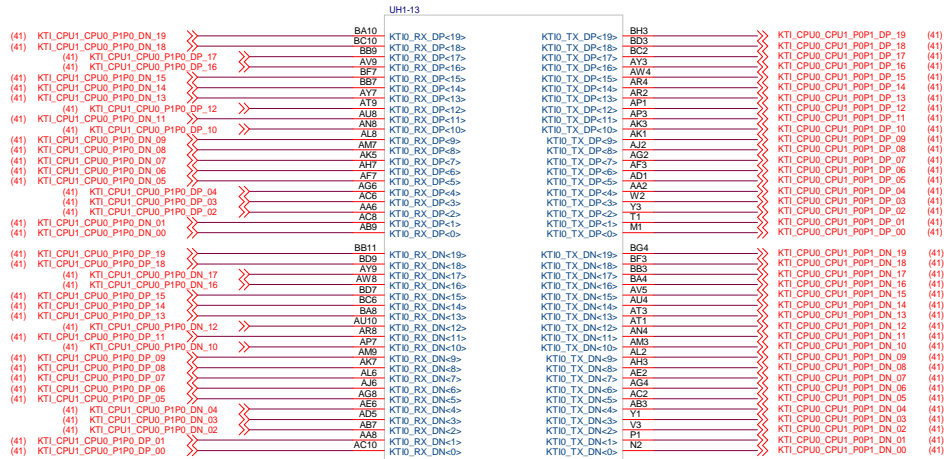


## DDR4\_CHF



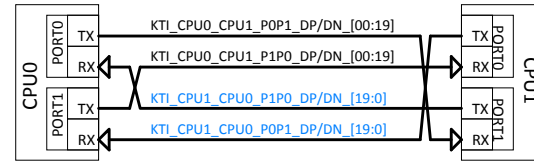




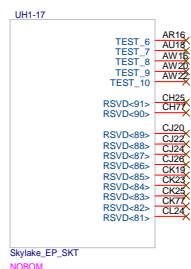


## KTI CPU0 Polarity Inversion

Lane Net Name	CPU0 Pin Name	CPU1 Pin Name	Polarity Inversion on Lane
KTI_CPU1_CPU0_P0P1_[DP/DN]_[19:00]	KTI0_RX_DP/DN[19:0]	KTI1_TX_DP/DN[19:0]	0,1,4,6,8,11,12,13,15,16,19
KTI_CPU1_CPU0_P1P0_[DP/DN]_[19:00]	KTI1_RX_DP/DN[19:0]	KTI0_TX_DP/DN[19:0]	0,1,5,6,7,8,9,11,13,14,15,18,19



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Yellow Key

PE36473-01DA1-1H

Black Key

PE36473-01DA2-1H

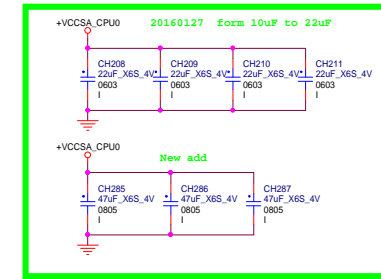
## xxx / H37268-003





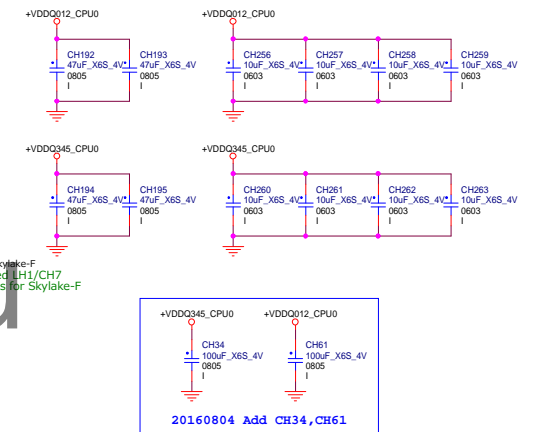
## CPU0 PVCCSA VR Decoupling Caps

<CAD> PLACE ALL AT TOP LAYER AT SOCKET CAVITY



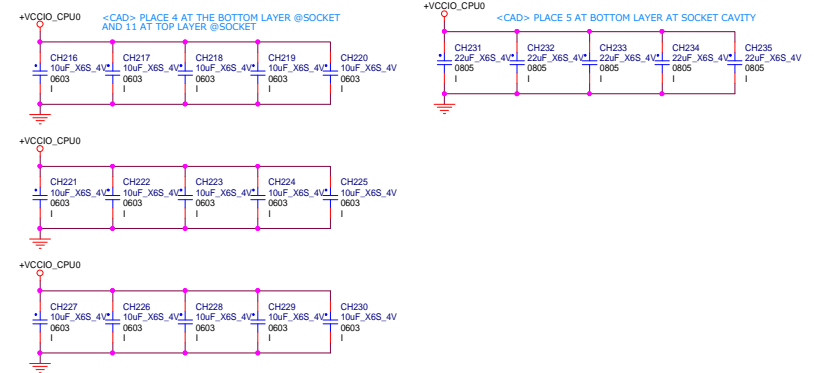
## PVDDQ\_ABCDEF\_CPU0 VR Decoupling Caps

<CAD> PLACE ALL AT THE SOCKET CAVITY



## CPU0 PVCCIO Decoupling Caps

<CAD> PLACE 4 AT THE BOTTOM LAYER @SOCKET AND 11 AT TOP LAYER @SOCKET

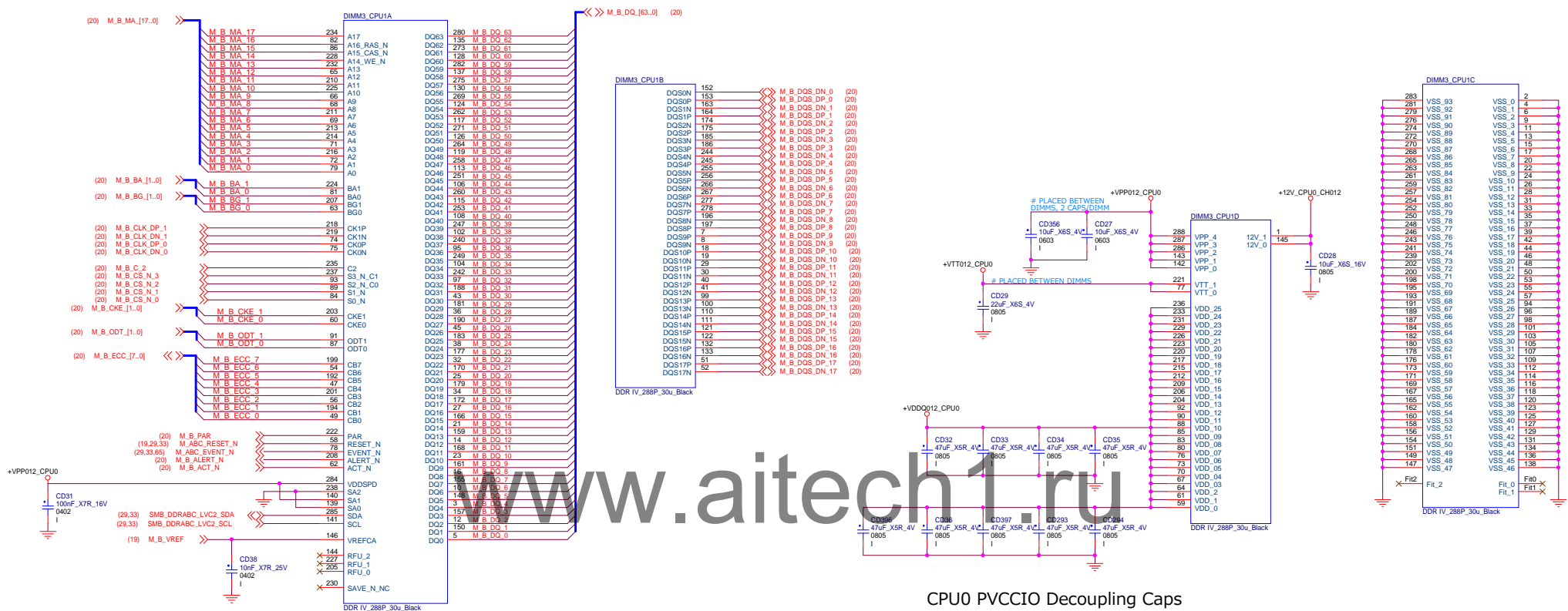


[illegible]



[illegible]

## DDR4 DIMM3 CPU0.CHB.D0



## CPU0 PVCCIO Decoupling Caps

# PLACE 4 BETWEEN DIMMS AND 3  
AT THE DIMM FIELD @SOCKET

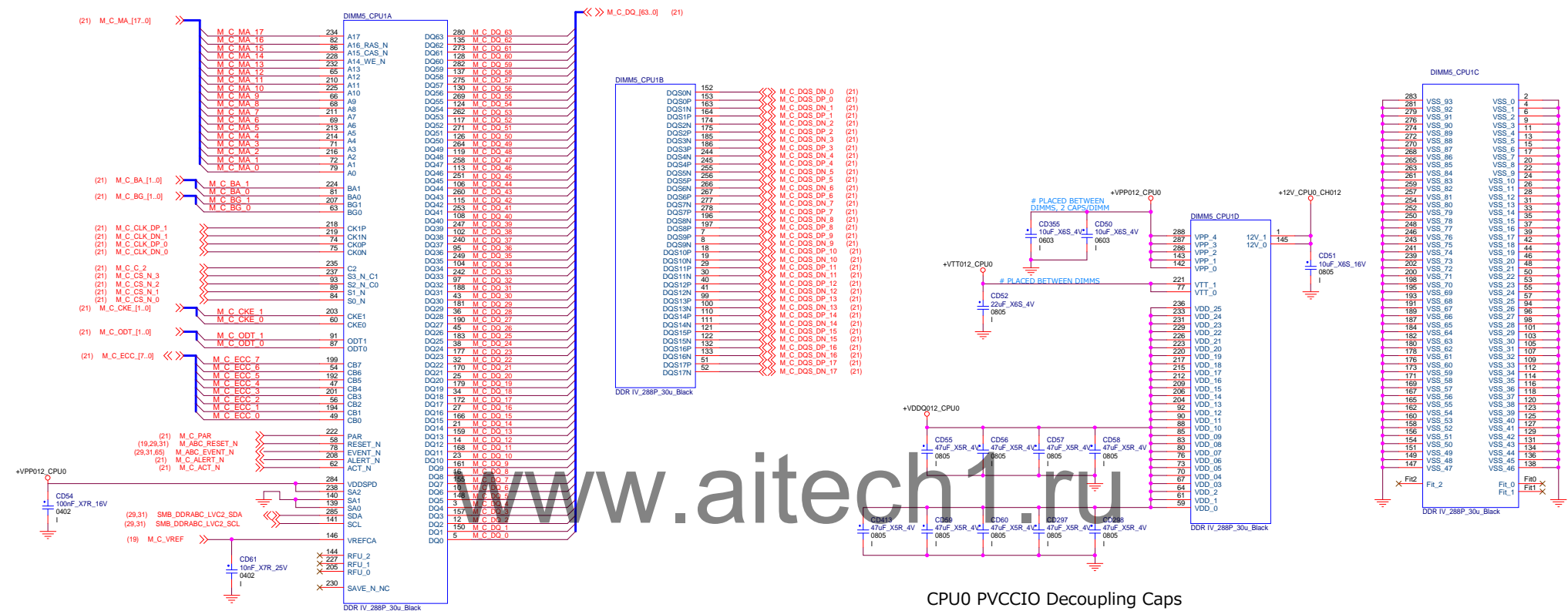
CRB -> 22uF x 8 / Avalon7 -> 46uF x 6







## DDR4 DIMM1 CPU0.CHC.D0



## CPU0 PVCCIO Decoupling Caps

# PLACE 4 BETWEEN DIMMS AND 3  
AT THE DIMM FIELD @SOCKET

CRB -> 22uF x 8 / Avalon7 -> 46uF x 6

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TITLE	DDR4 DIMM1 CPU0.CHC.D0
DWG NO.	MATIRA 5
DATE	Thursday, June 20, 2013

COMPRESS  
IMAGE

SA[2:0] = 101 SPD = 0xAA TSOD = 0x3A
--------------------------------------------

## DDR4 DIMM11 CPU0.CHC.D1

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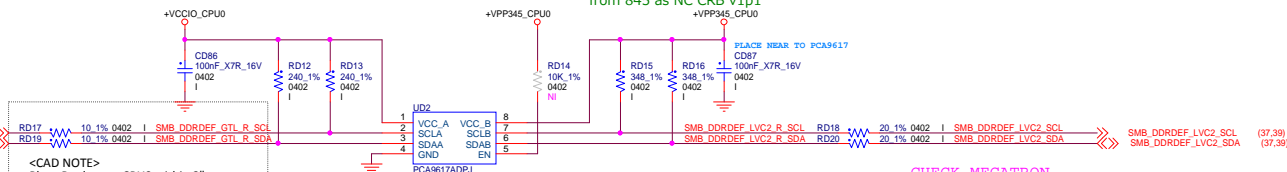
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## DDR4 DIMM6 CPU0.CHD.D0




CRB -> 22uF x 8 / Avalon7 -> 46uF x 6

CRB -> 22uF x 8 / Avalon7 -> 46uF x 6



CHECK MEGATRON

COMPRESS  
IMAGE

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## DDR4 DIMM4 CPU0.CHE.D0



CRB -> 22uF x 8 / Avalon7 -> 46uF x 6



## DDR4 DIMM2 CPU0.CHF.D0



# PLACE 4 BETWEEN DIMMS AND 3  
AT THE DIMM FIELD @SOCKET

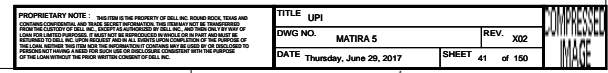
CRB -> 22uF x 8 / Avalon7 -> 46uF x 6




SA[2:0] = 101  
SPD = 0xAA  
TSOD = 0x3A

DDR4 DIMM12 CPU0.CHF.D1

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<b>DWG NO.</b> MATRIZA 5		<b>REV.</b> X02			
<b>DATE</b> Thursday, June 29, 2017		<b>SHEET</b> 42 of 150			


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<p><b>DWG NO.</b> MATRISA 5</p>		<p><b>REV.</b> X02</p>	
<p><b>DATE</b> Thursday, June 29, 2017</p>		<p><b>SHEET</b> 46 of 150</p>	


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		<b>DWG NO.</b> MATRIZA 5		<b>REV.</b> X02			
		<b>DATE</b> Thursday, June 29, 2017		<b>SHEET</b> 47 of 150			


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
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
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
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
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
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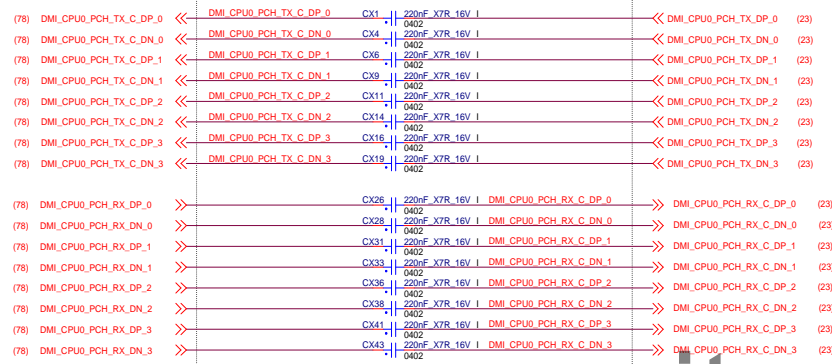
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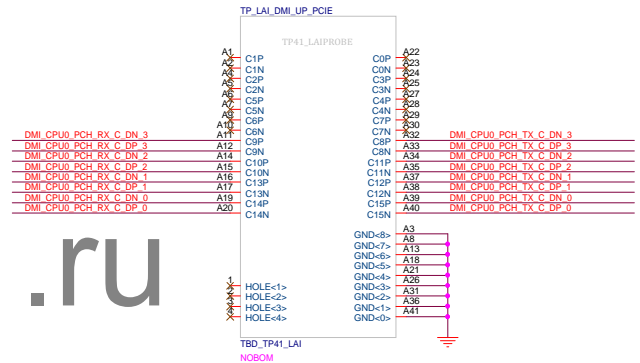
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DMI

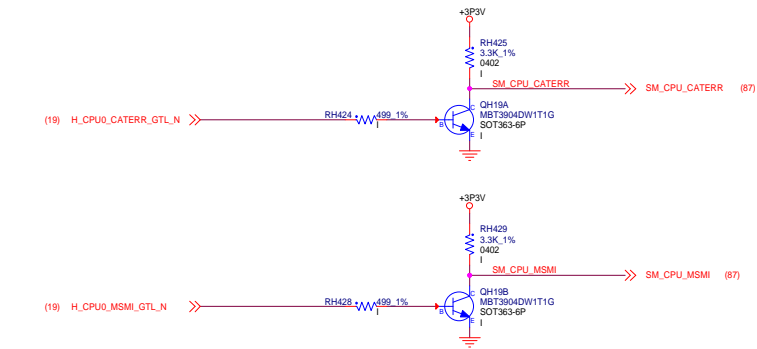
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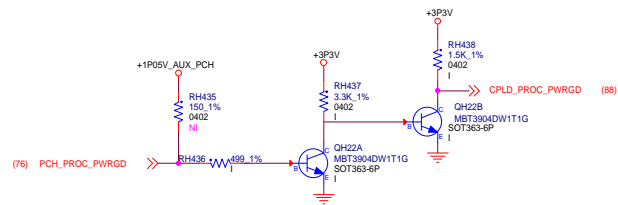
### DMI/UPLINK LAI Connector



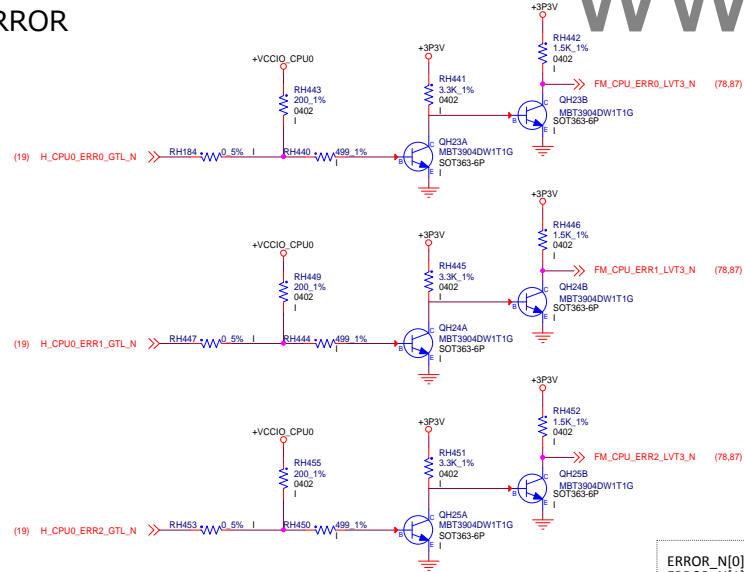
CRTERR / MSMI / EAR / CPU PG



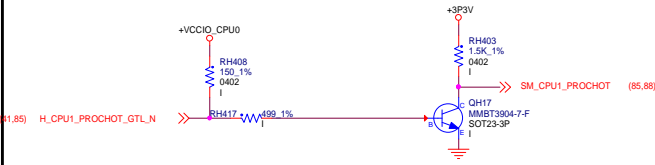
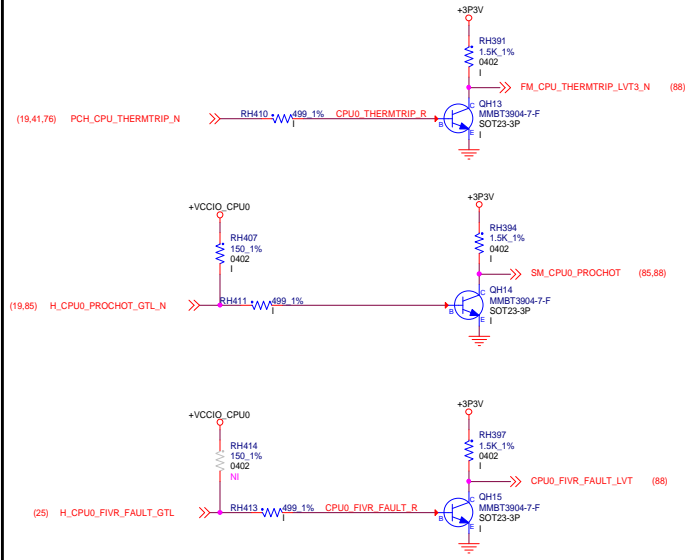
20160315 del FM\_CPU0\_EAR\_G\_N,FM\_CPU1\_EAR\_G\_N,FM\_CPU\_EAR\_LVT\_N peripheral component



ERROR



ERROR\_N[0] = ECE/ PCH  
ERROR\_N[1] = ECE/ PCH  
ERROR\_N[2] = ECE







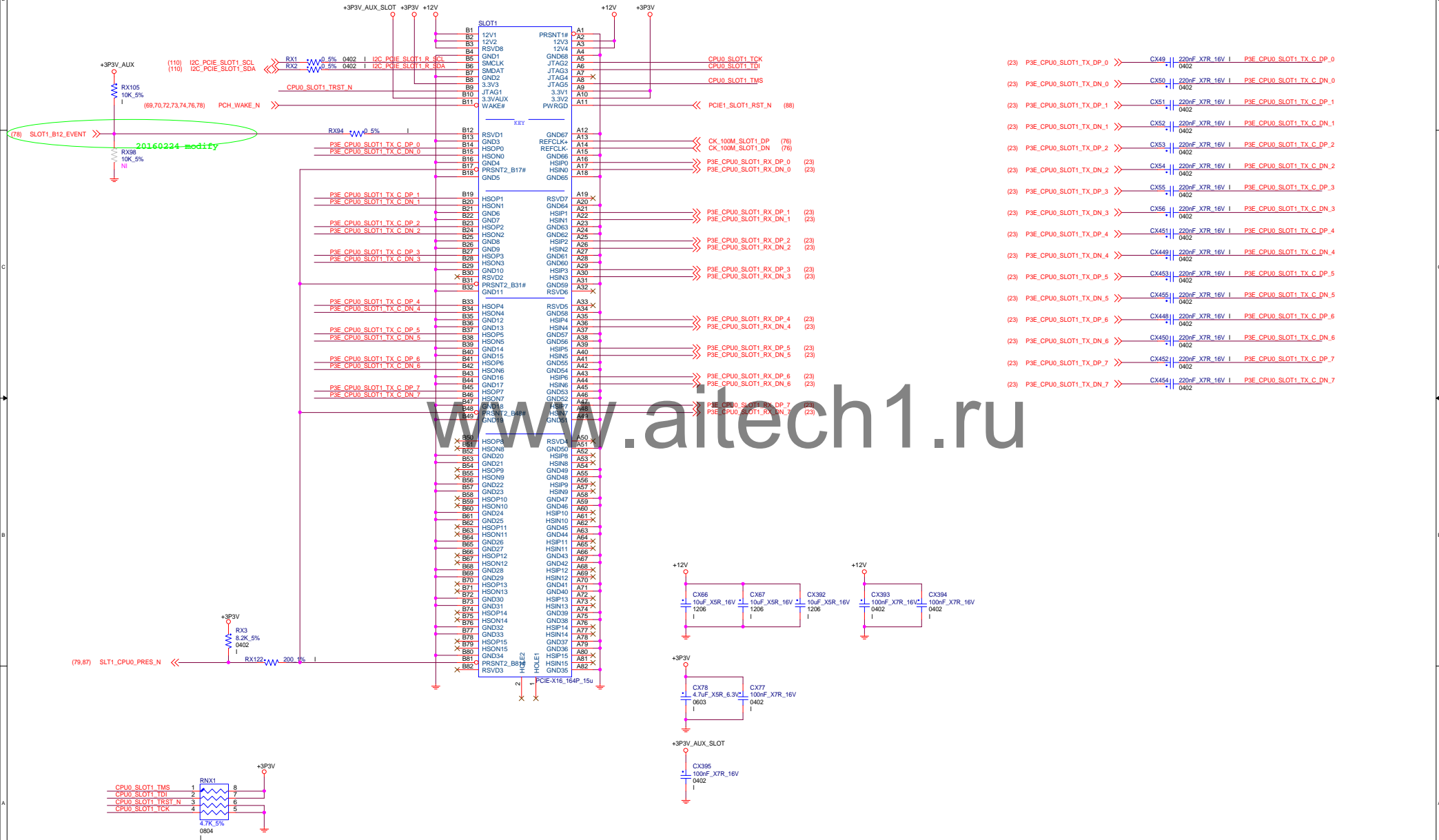
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## LPC CLOCK BUFFER

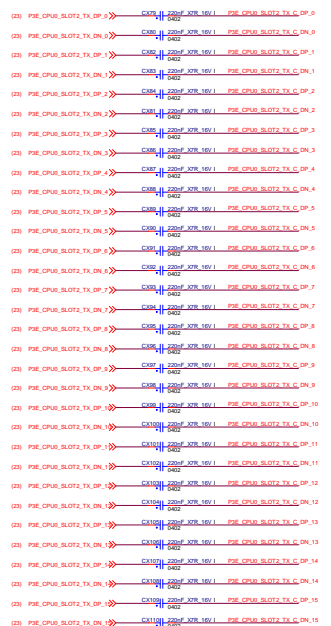
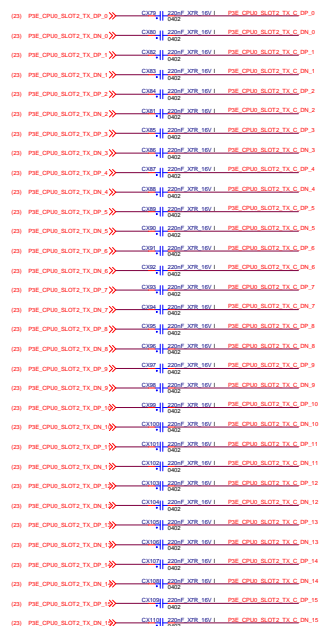
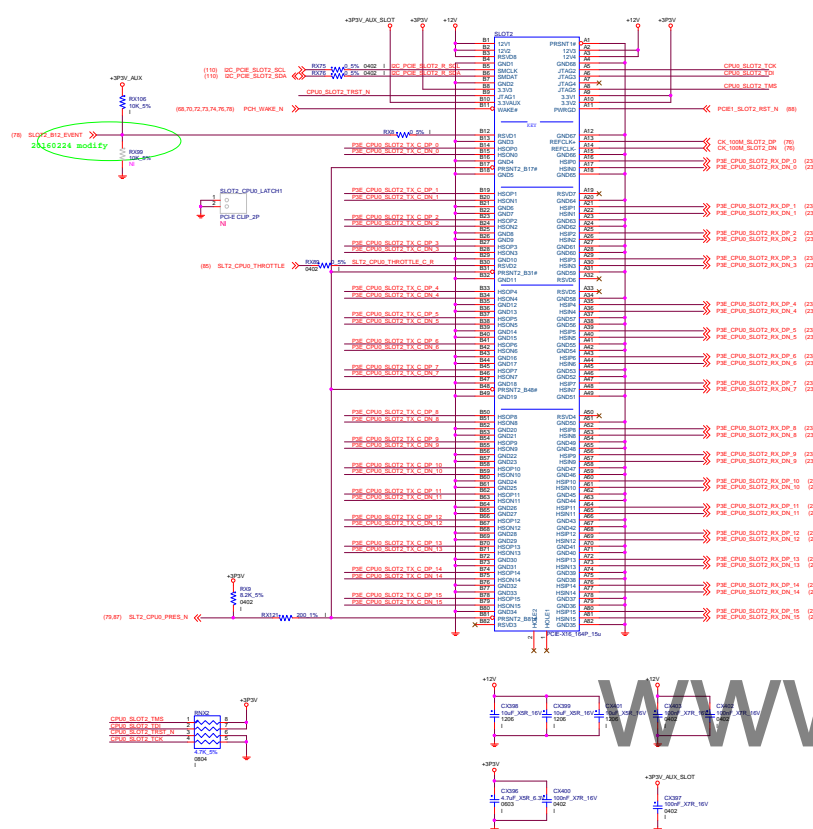
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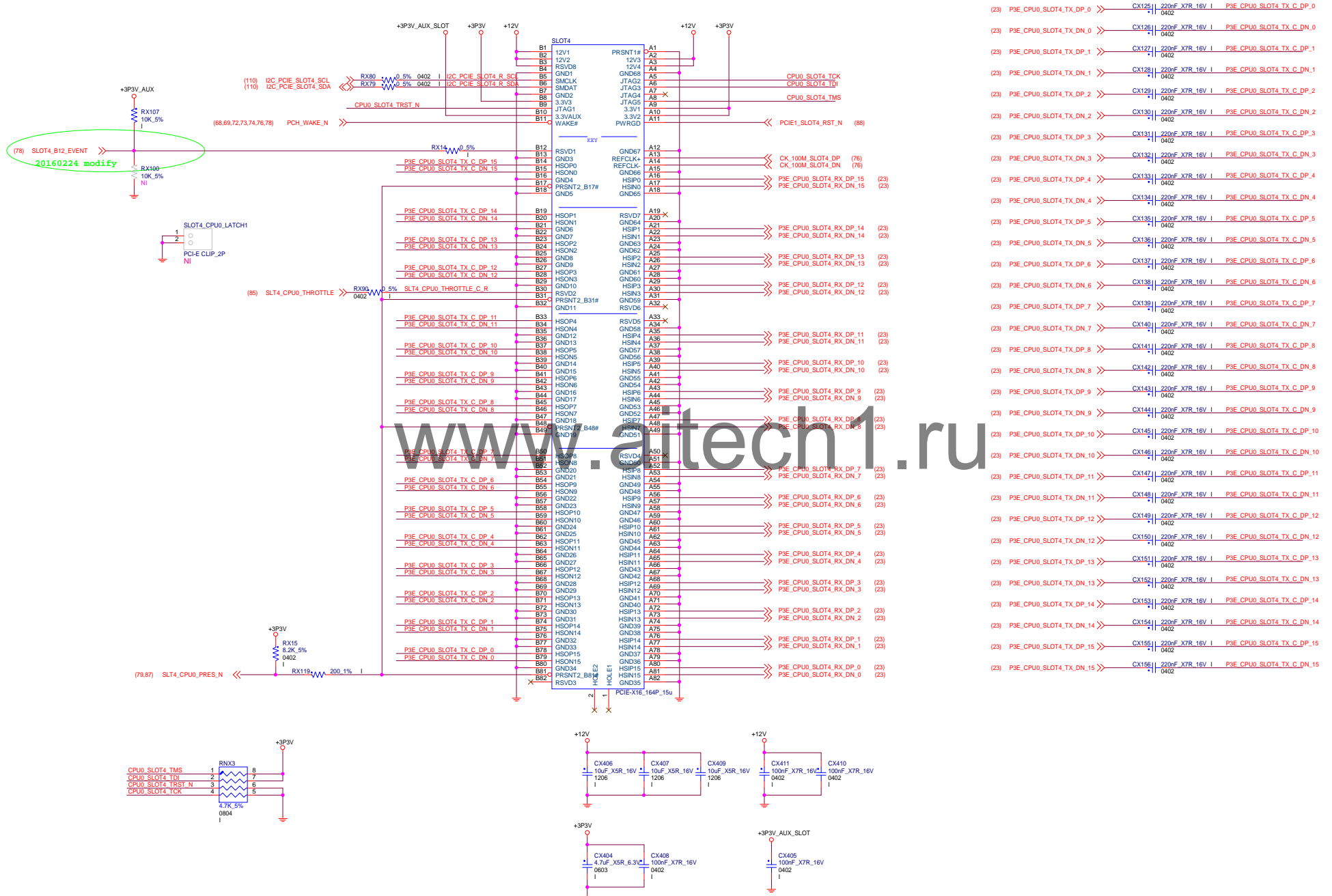
# PCIE x8 SLOT1 (CPU0 WIRED 8X GEN3)



## PCIE x16 SLOT2 (CPU0 WIRED 16X GEN3)



## PCIE x16 SLOT4 (CPU0 WIRED 16X GEN3)

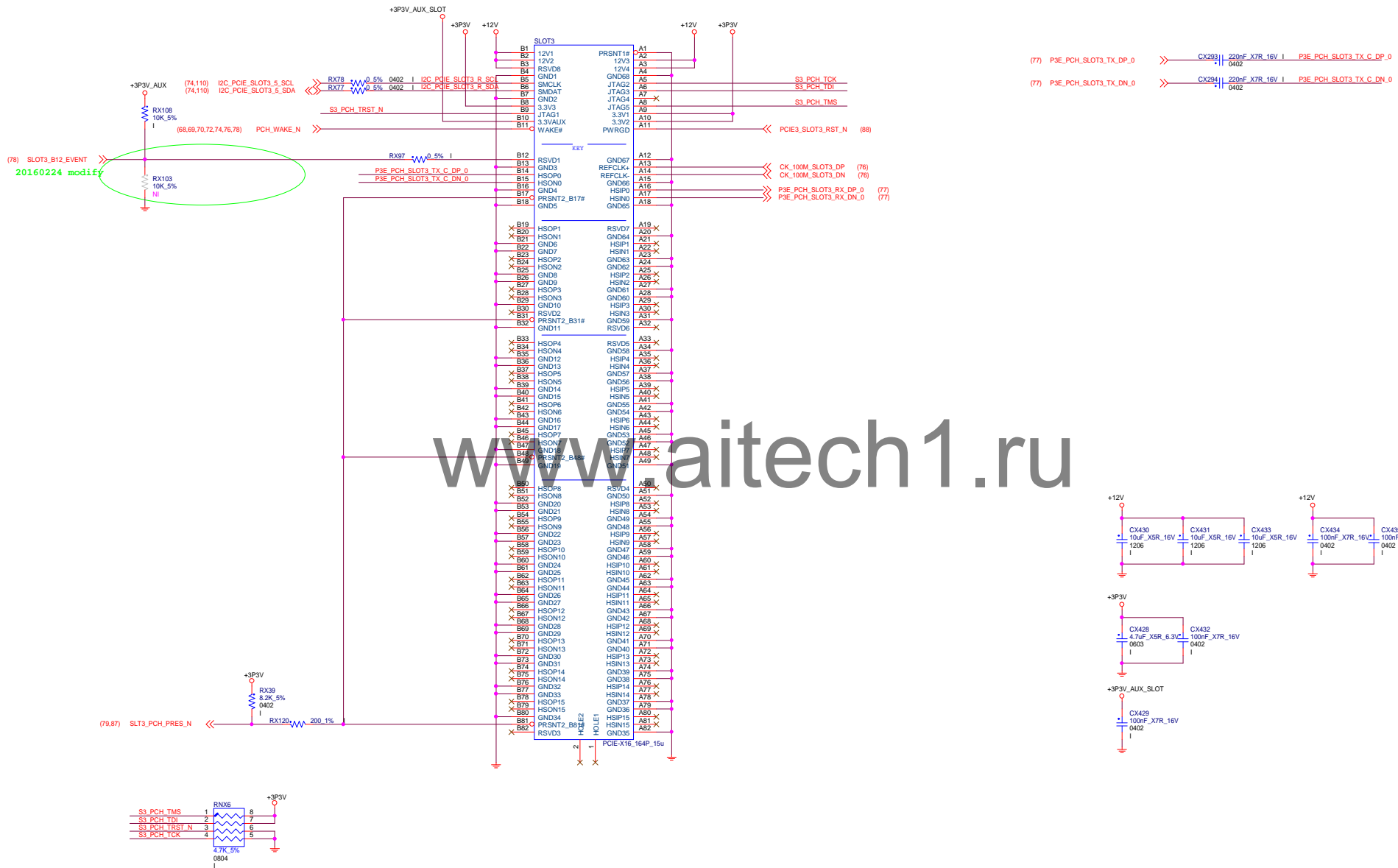




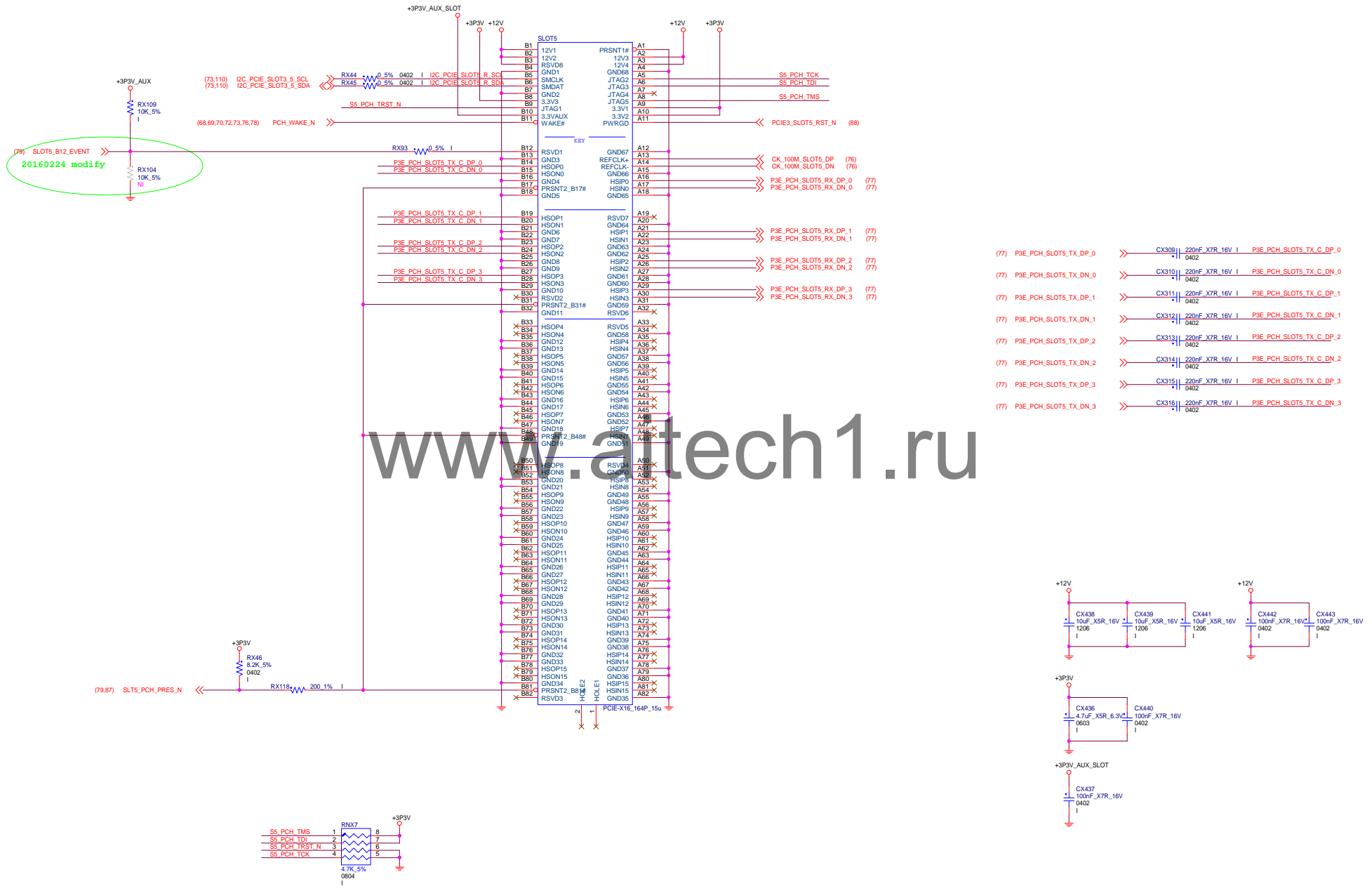




# PCIE x16 SLOT3 (PCH WIRED 1X GEN3)



# PCIE x16 SLOT5 (PCH WIRED 4X GEN3)



5	4	3	2	1
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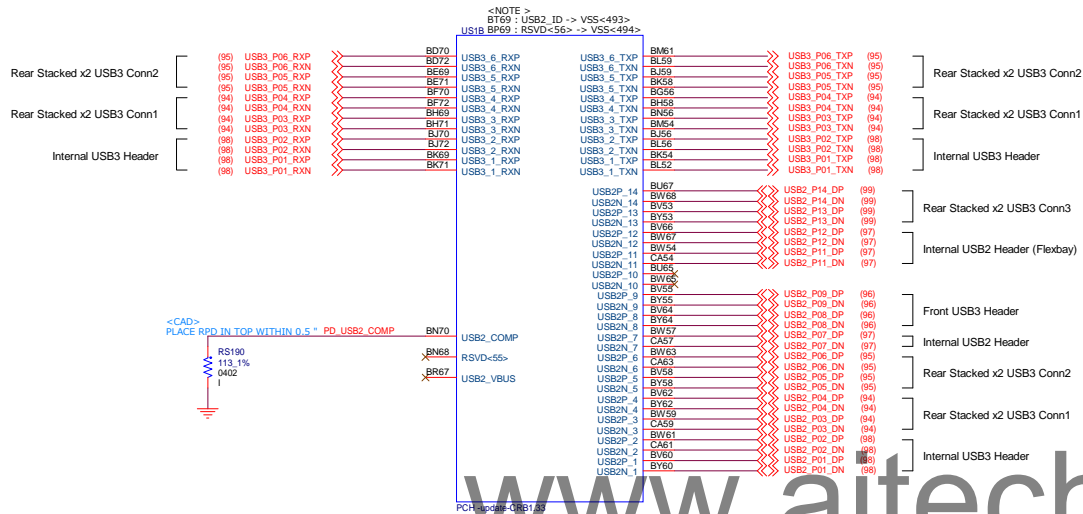
COMPRESSED  
IMAGE

The diagram illustrates the PCH (Platform Controller Hub) symbol and its connections. It includes various pins and their connections to external components like resistors, capacitors, and other chips. The diagram is divided into several sections: PCH update-CRB1.33, PCH update-CRB1.33, PCH update-CRB1.33, PCH update-CRB1.33, PCH update-CRB1.33, PCH update-CRB1.33, PCH update-CRB1.33, PCH update-CRB1.33, PCH update-CRB1.33, PCH update-CRB1.33. The diagram includes a large watermark 'www.aitech1.ru' across the center.

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TITLE PCH CLOCKLAN/JTAG		COMPRESSED IMAGE
DWG NO. MATIRA 5	REV. X02	
DATE Thursday, June 29, 2017	SHEET 76 of 150	

# COMPRESSED IMAGE



### USB Port Mapping Table

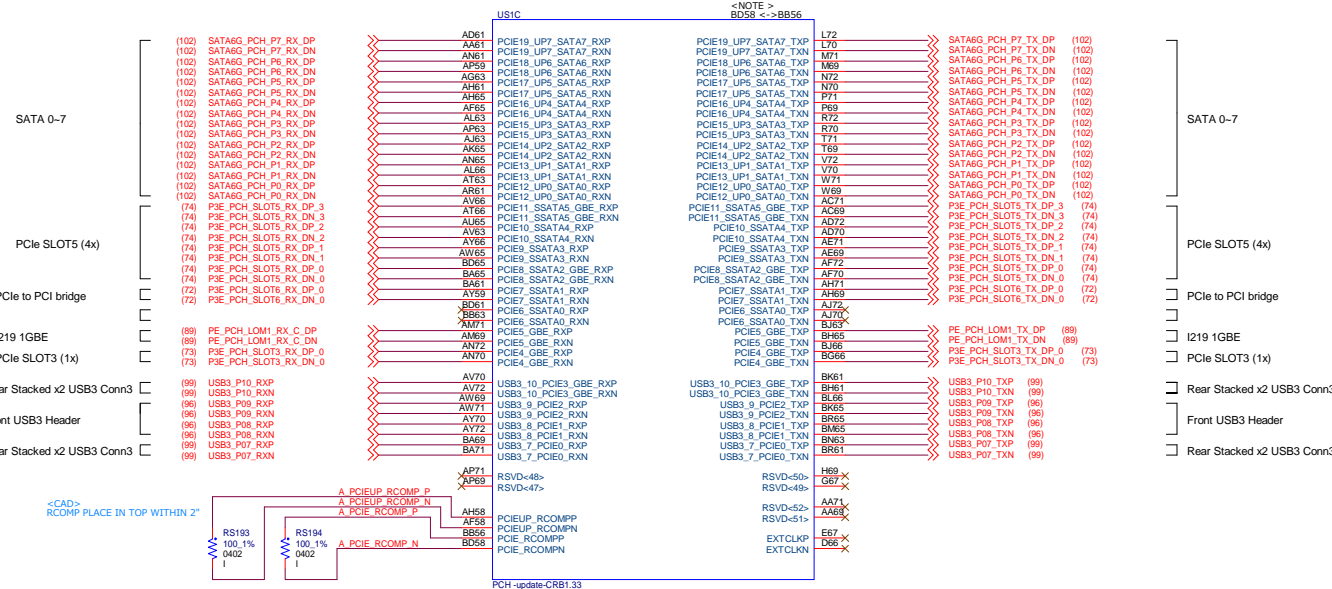
USB3	USB2	OC#	Location
1-2	1-2	0-1	Internal USB3 Header
3-4	3-4	2-3	Rear Stacked x2 USB3 Conn1
5-6	5-6	4-5	Rear Stacked x2 USB3 Conn2
7	7	6	Internal USB2 Conn. (TypeA)
8-9	8-9	6	Front USB3 Header
11-12	11-12	7	Internal USB2 Header (Flexbay)
7-10	13-14		Rear Stacked x2 USB3 Conn3

### SATA Port Mapping Table

SATA3	SSATA3	Location
0-3		SATA0-SATA3
4-7		SATA4-SATA7

### PCIE Port Mapping Table

PCIe3	Function	Location
0	Y	N/A
1-2		Internal USB3 Header
3		N/A
4	Y	PCIe SLOT 3 (1x)
5	Y	I219 1GBE
6		N/A
7	Y	PCIe to PCI bridge
8-11	Y	PCIe SL OT5 (4x)



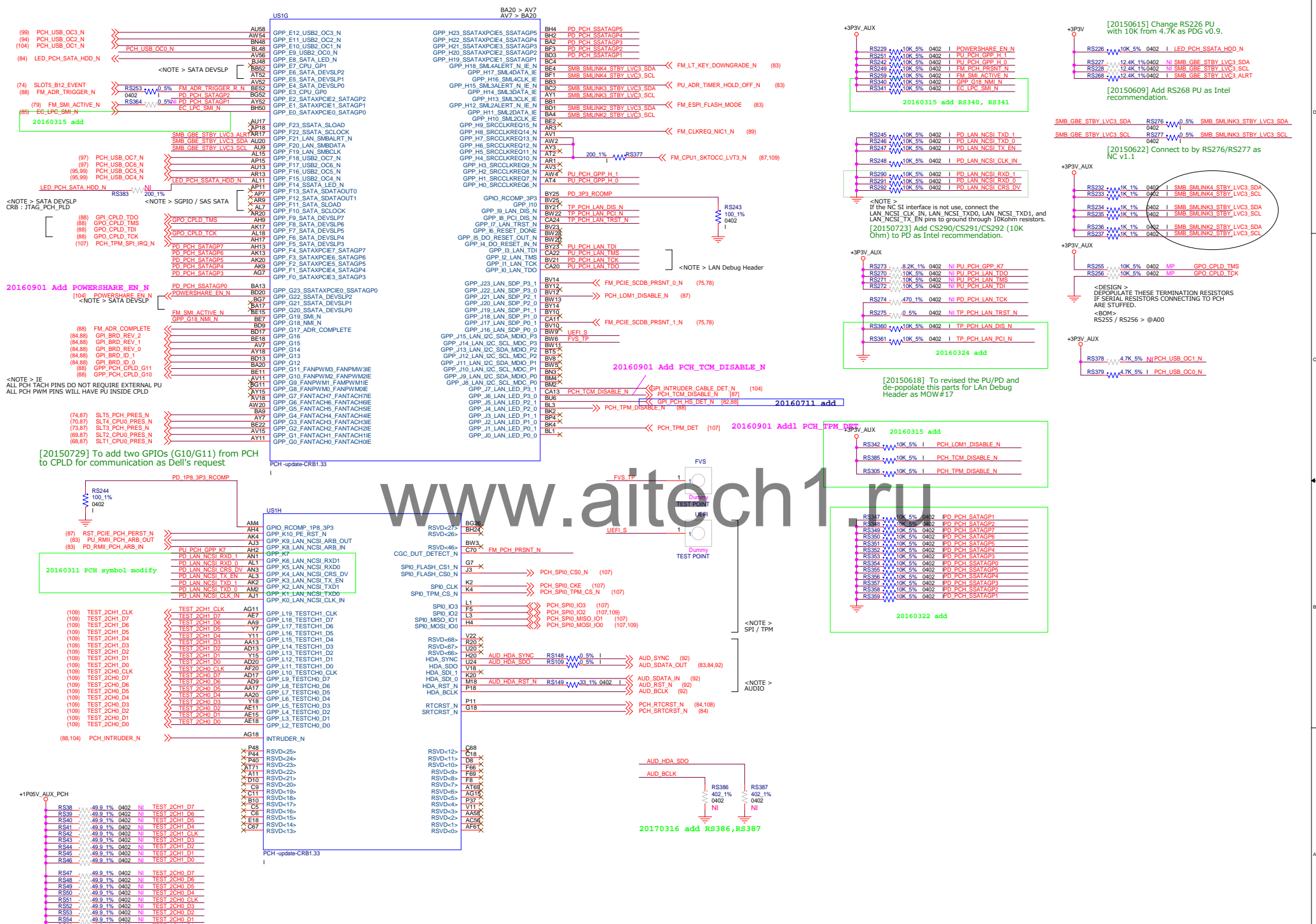
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TITLE		PCH USB/PCIE/SATA	
DWG NO.		MATIRA 5	REV. X02
DATE		Thursday, June 29, 2017	SHEET 77 of 150

COMPRESSED  
IMAGE



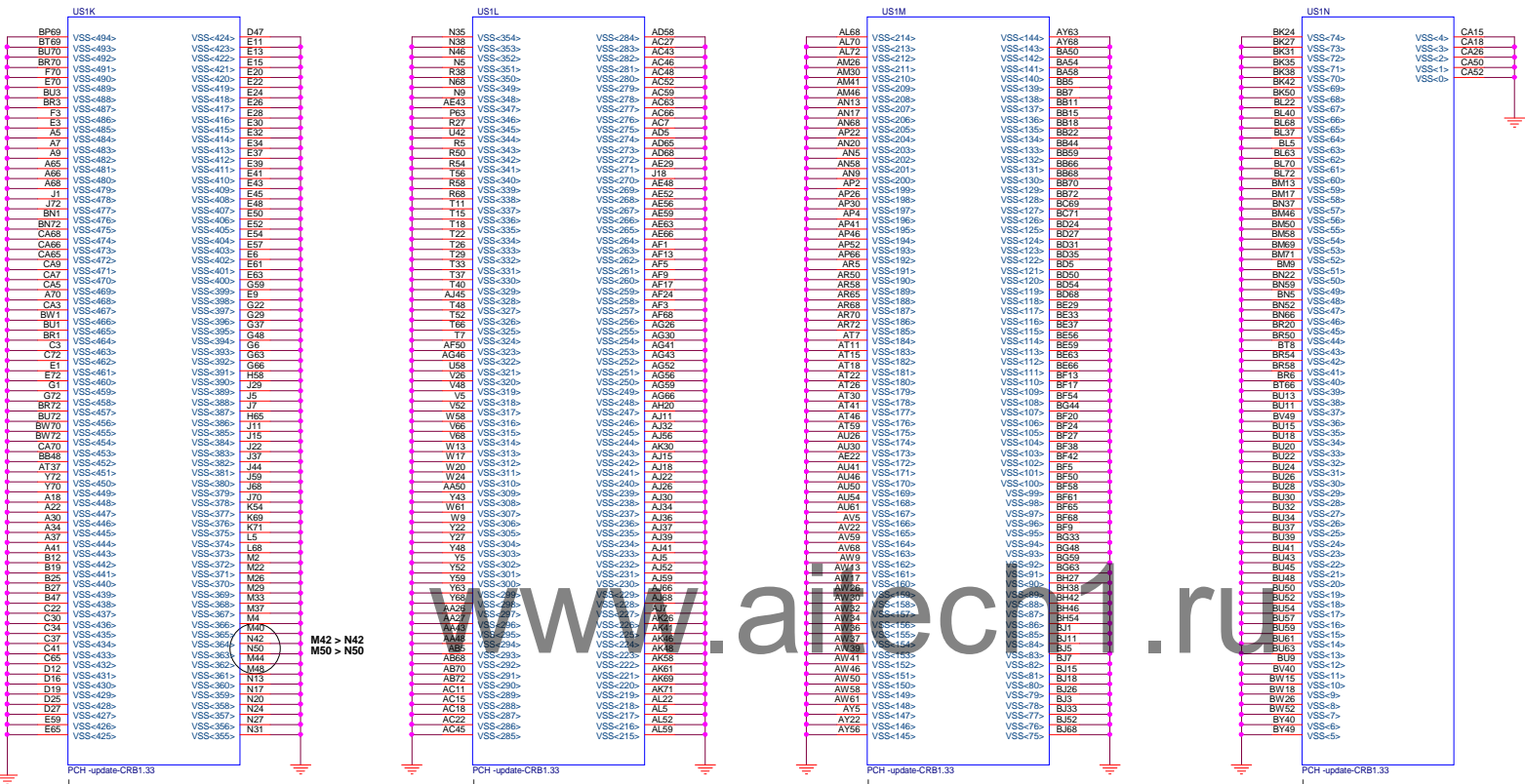










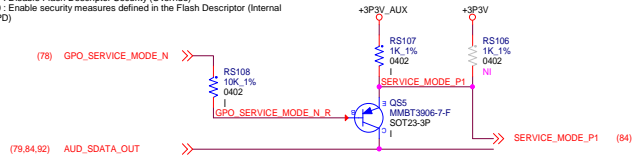


## PCH HEATSINK DET



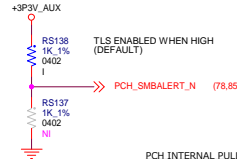
## SERVICE MODE JUMPER

(ME FW Override Jumper)  
1: Disable Flash Descriptor Security (Override)  
0: Enable security measures defined in the Flash Descriptor (Internal PD)



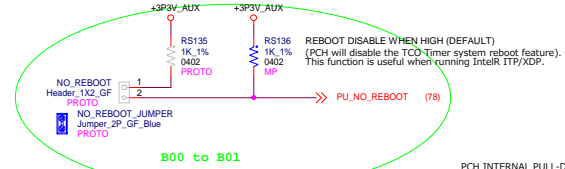
FLASH SECURITY OVERRIDE  
PCH INTERNAL PULL-DOWN.  
1 > FLASH SECURITY OVERRIDE  
ENABLE  
0 > FLASH SECURITY OVERRIDE  
DISABLE (DEFAULT)

## TLS CONFIDENTIALITY



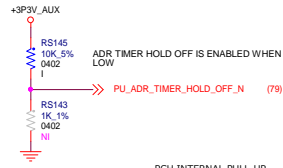
PCH INTERNAL PULL-DOWN.  
1 > TLS ENABLED  
0 > TLS DISABLE

## NO REBOOT STRAP



PCH INTERNAL PULL-DOWN.  
1 > Enable (No Reboot) mode.  
0 > Disable (No Reboot) mode.

## ADR TIMER OFF



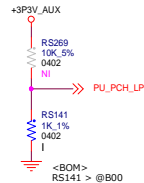
PCH INTERNAL PULL-UP.  
1 > ADR Timer Hold off is not enabled.  
0 > ADR Timer Hold off is enabled.

## ESPI FLASH SHARING MODE

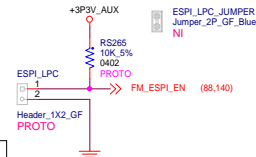


PCH INTERNAL PULL-DOWN.  
1 > SLAVE ESPI FLASH SHARING  
0 > MASTER ESPI FLASH SHARING  
(DEFAULT)

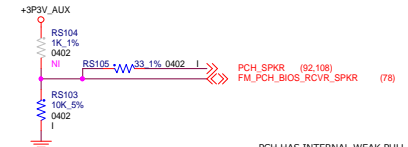
## ESPI OR LPC



The internal pull-down is disabled after RSMRST# de-asserts.  
1 > eSPI functionality is selected.  
0 > LPC functionality is selected.

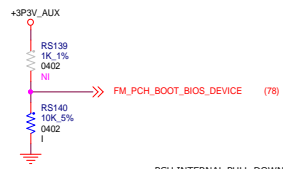


## TOP SWAP MODE STRAP



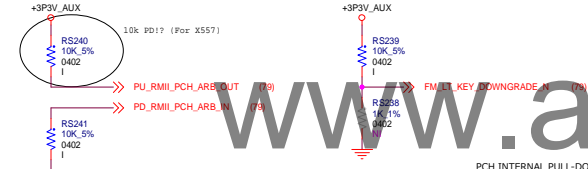
PCH HAS INTERNAL WEAK PULL-DOWN.  
1 > TOP SWAP ENABLED  
0 > TOP SWAP DISABLED (DEFAULT)

## BOOT BIOS DEVICE



PCH INTERNAL PULL-DOWN.  
1 > LPC / ESPI  
0 > SPI (DEFAULT)

## D3COLD POWER STATE



PCH INTERNAL PULL-DOWN.  
1 > Aux power is available and the 10GbE LAN should support the D3COLD power state if enabled to do so.  
0 > D3COLD is not supported.

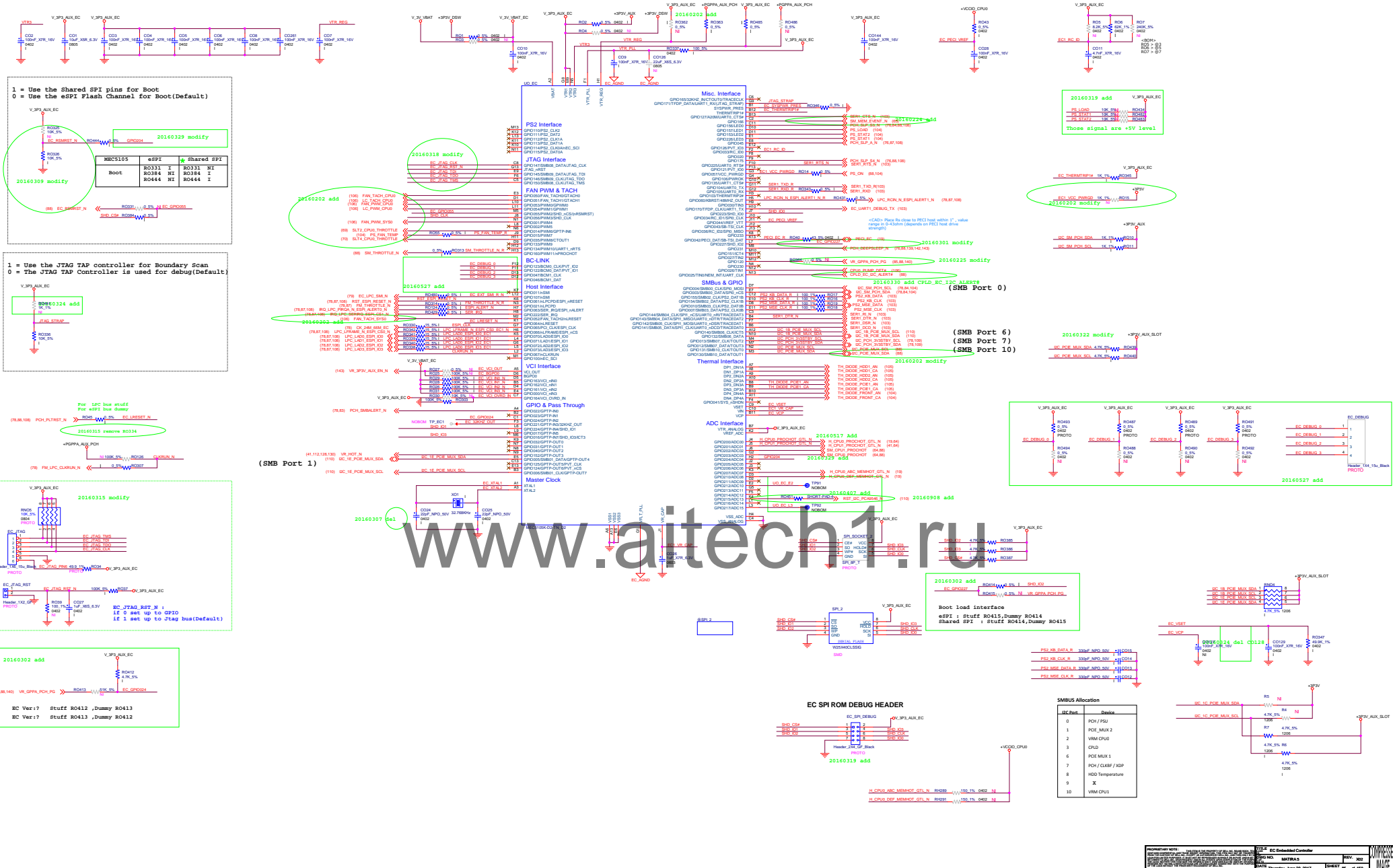
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TITLE STRAP  
DWG NO. MATIRA 5  
DATE Thursday, June 29, 2017  
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SHEET 63 of 150

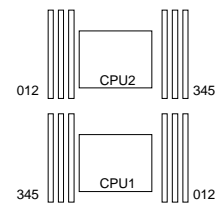
COMPRESSED  
IMAGE





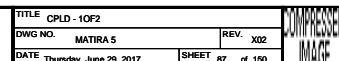
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20160309 del



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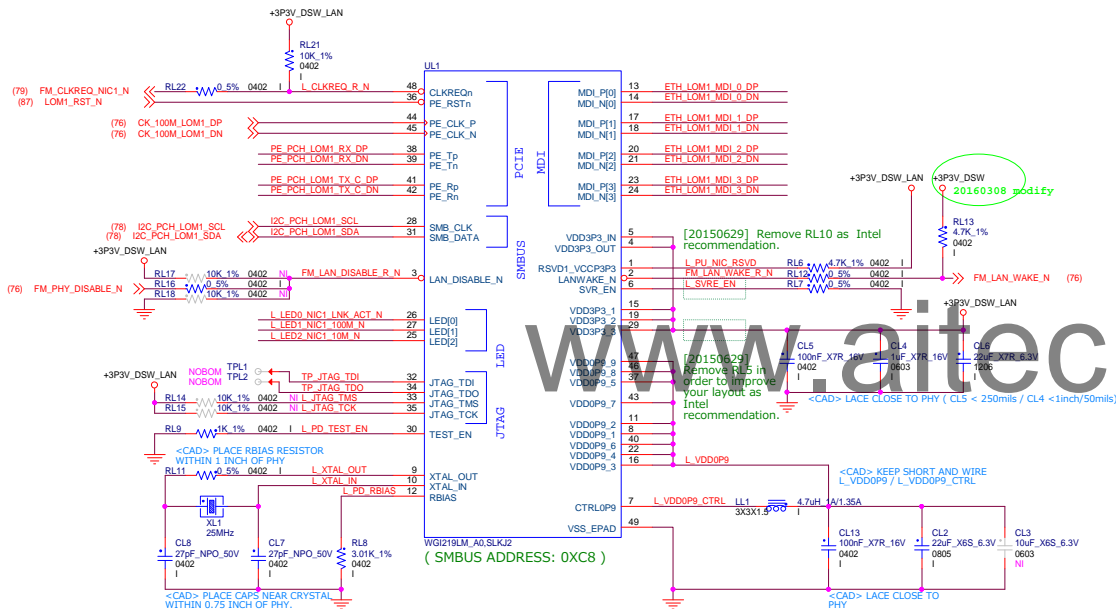
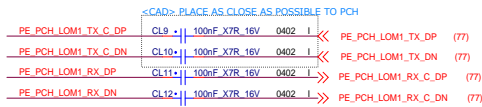
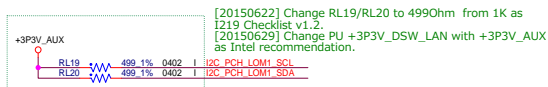
TITLE EC GPIO Expander		COMPRESSED IMAGE
DWG NO. MATIRA 5	REV. X02	
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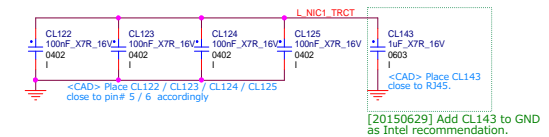
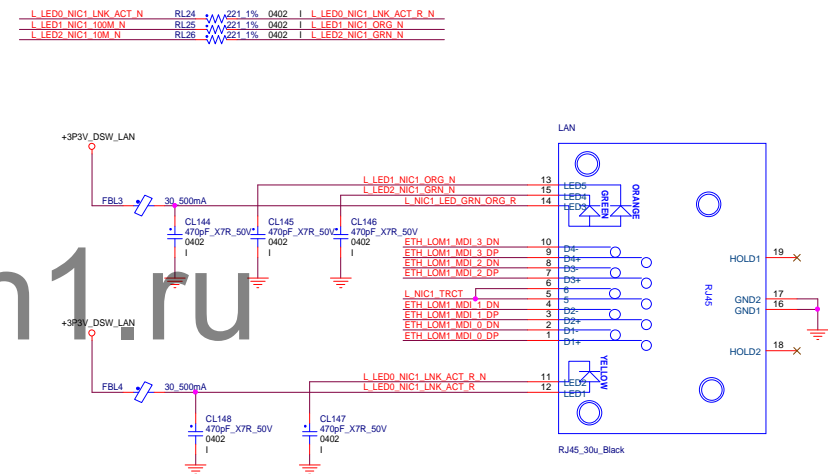
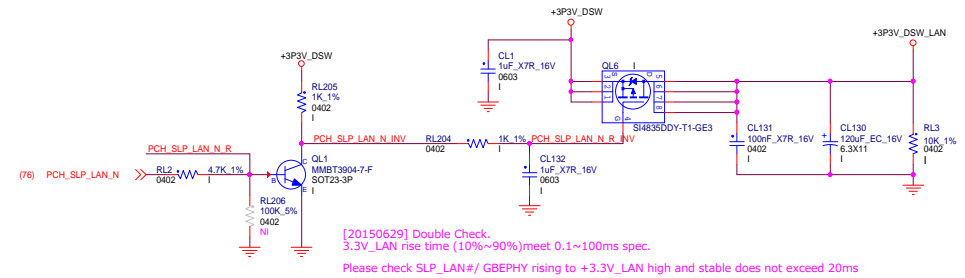





## Jacksonville / I219 (PHY)



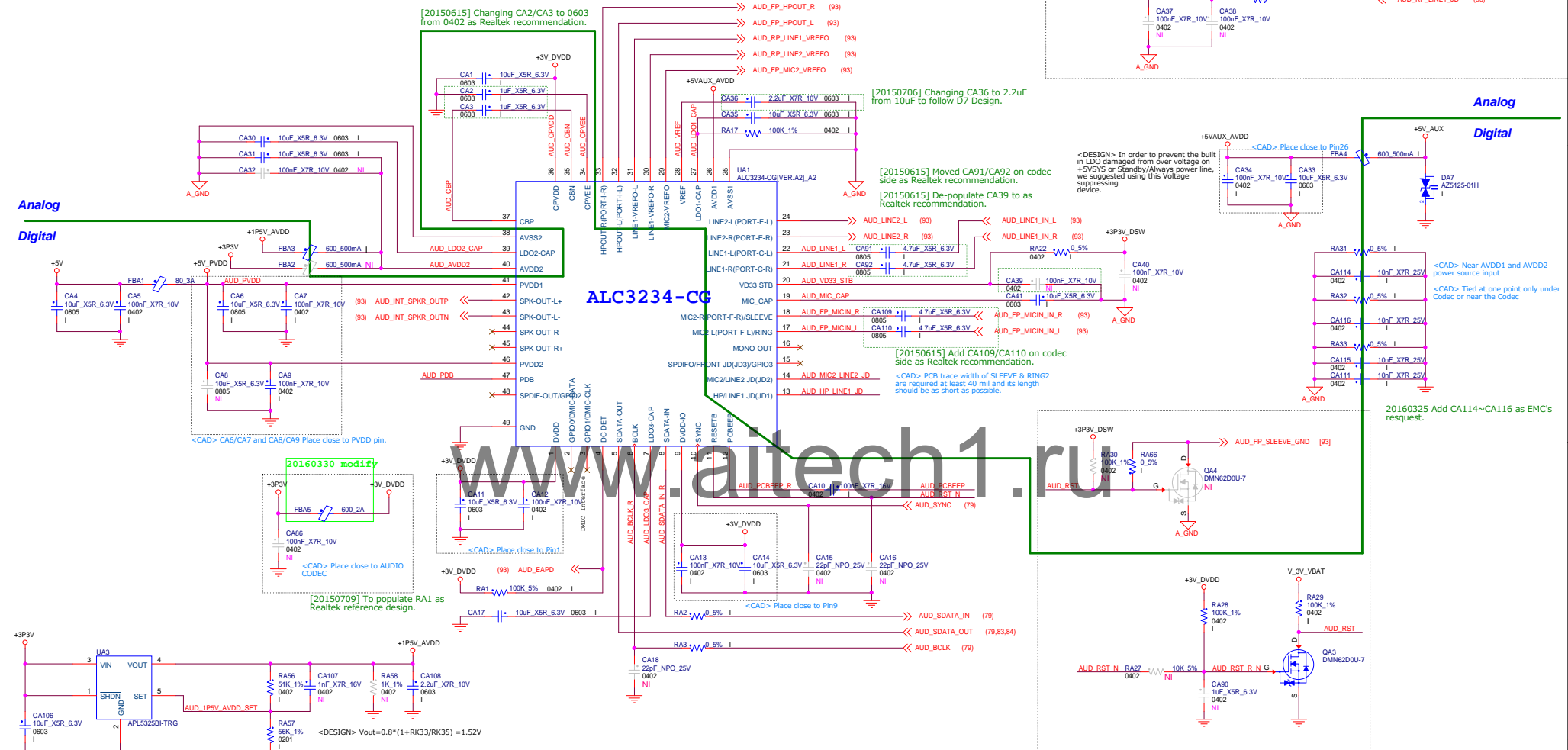
## I219 LOM Power



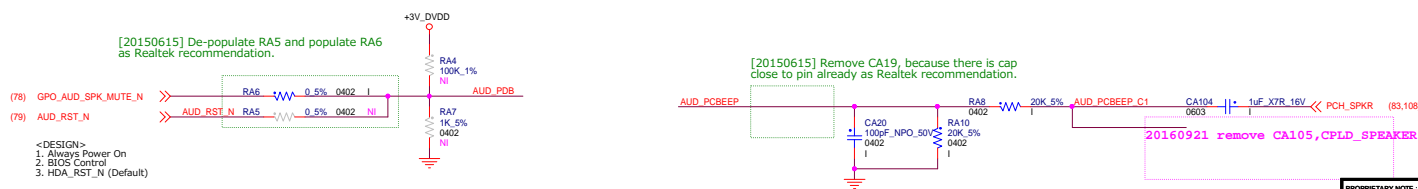
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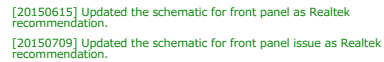
## Audio Codec



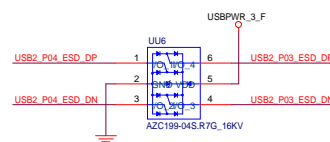
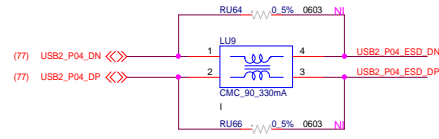
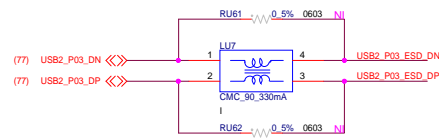
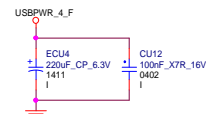
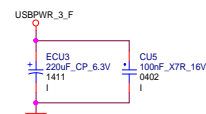
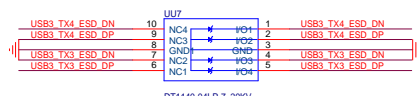
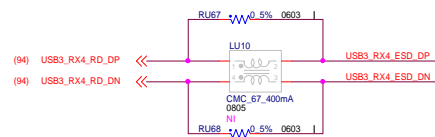
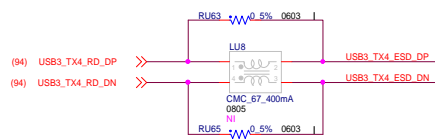
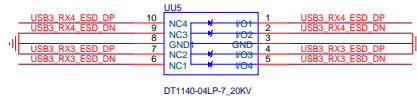
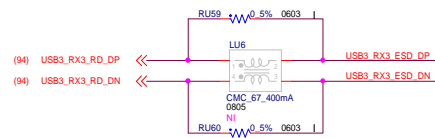
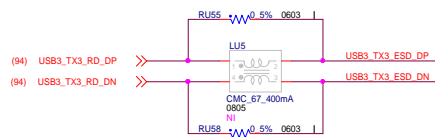
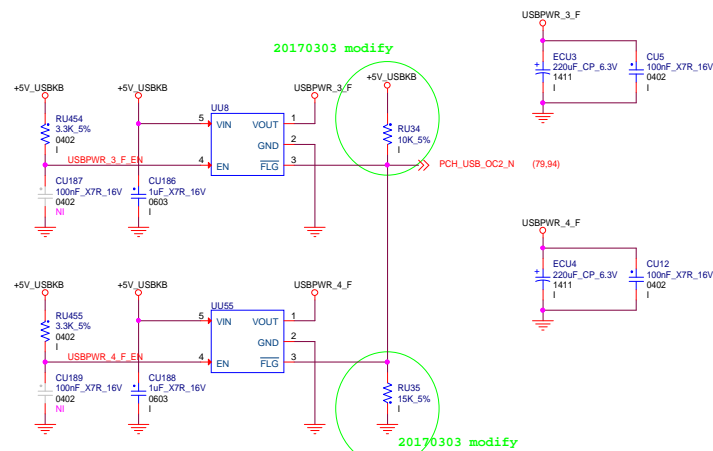
## Amplifier Power Down Options



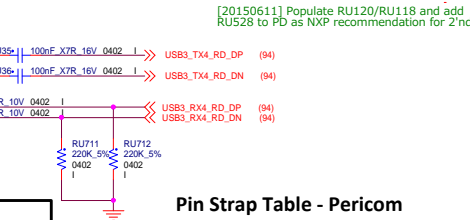
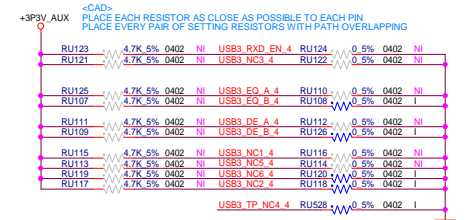
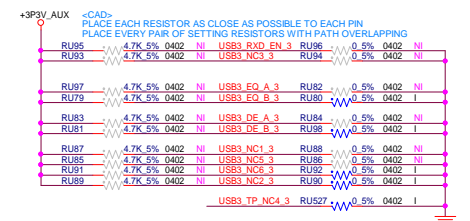
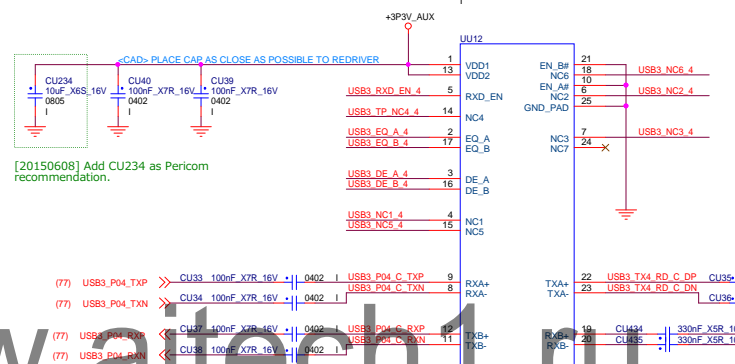
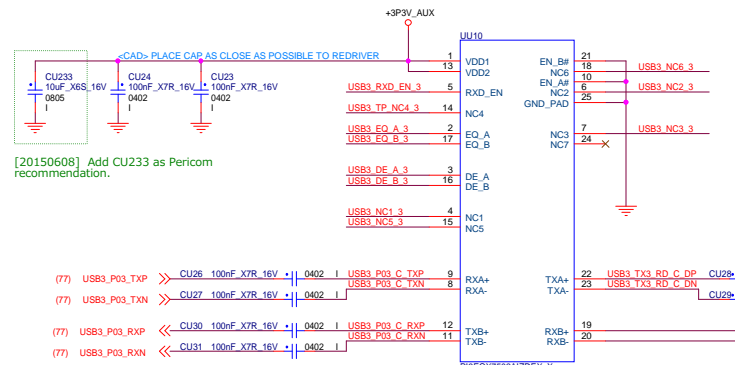
[20150709] Updated the schematic for Rear Panel as Realtek recommendation.

[illegible]

## Rear USB3.0 Connector 10F2

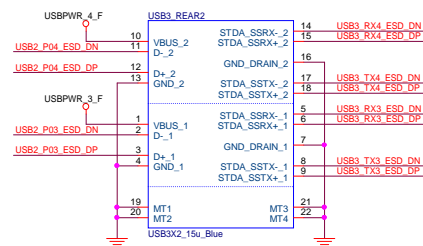


## USB3.0 REDRIVER



### Pin Strap Table - Pericom

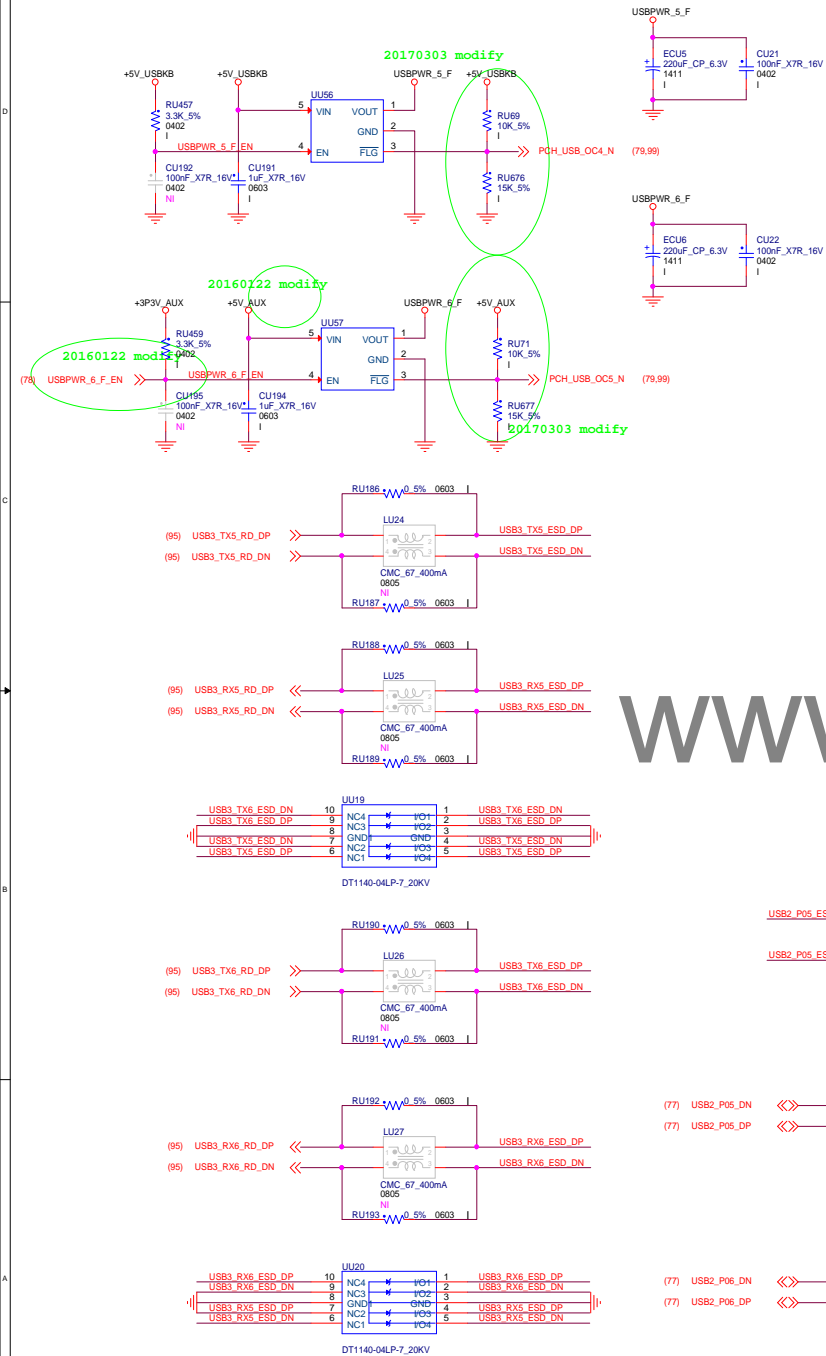
EQ_x	@2.5GHz	DE_x	
Pin#2	CHA	Pin#3	CHA
Pin#17	CHB	Pin#16	CHB
0	3dB	0	0dB
NC	6dB	NC	-3.5dB
1	9dB	1	-6dB



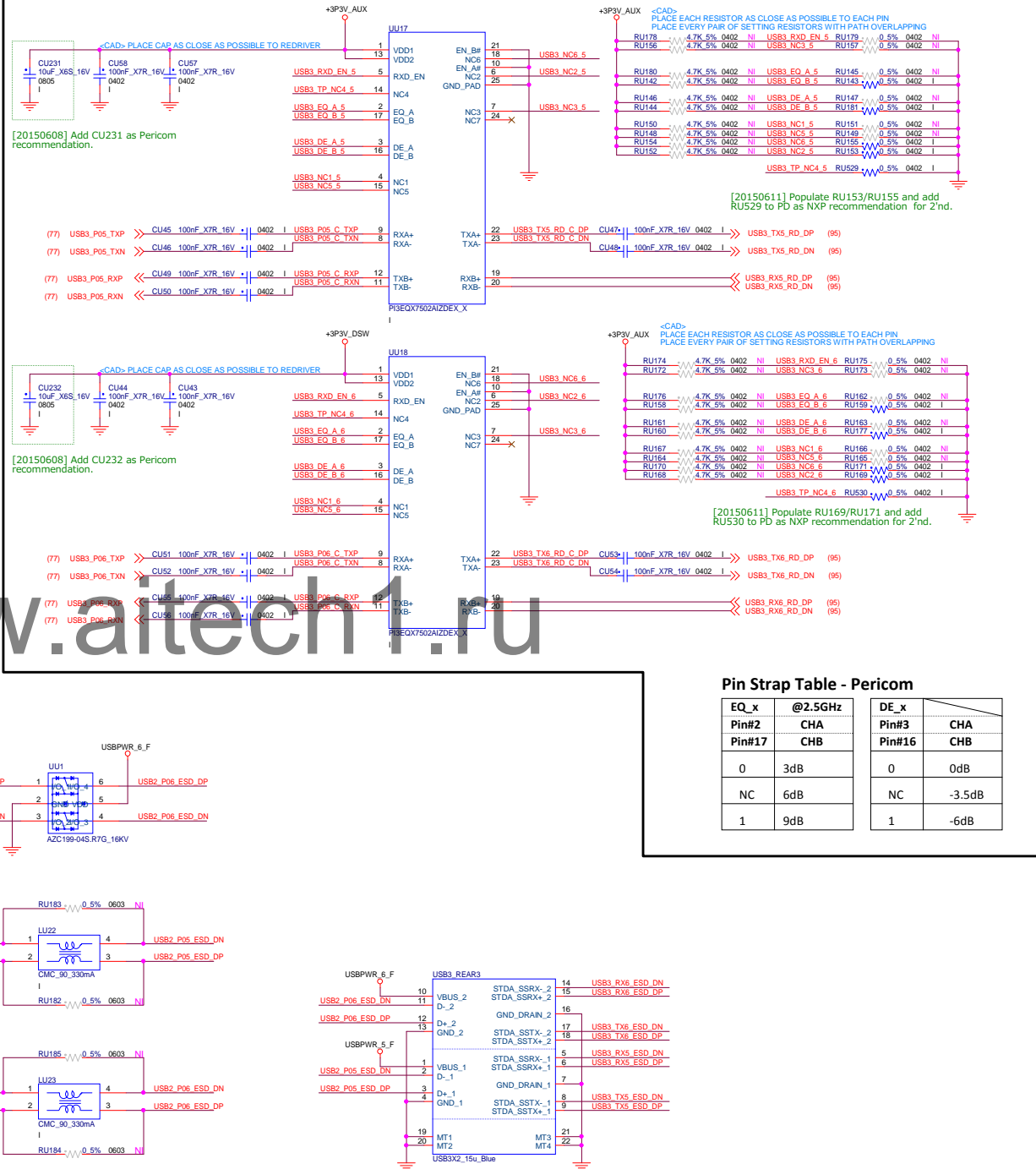
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TITLE		USB 3.0 Connector - 10F3	
DWG NO.		MATIRA 5	REV. X02
DATE		Thursday, June 29, 2017	SHEET 04 of 150

## Rear USB3.0 Connector 20F2



## USB3.0 REDRIVER



### Pin Strap Table - Pericom

EQ_x	@2.5GHz	DE_x	
Pin#2	CHA	Pin#3	CHA
Pin#17	CHB	Pin#16	CHB
0	3dB	0	0dB
NC	6dB	NC	-3.5dB
1	9dB	1	-6dB

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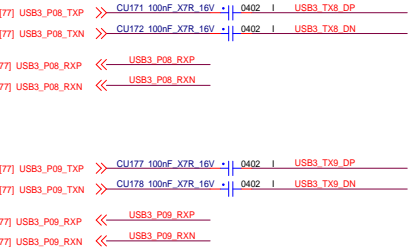
Front Panel USB3.0 Connector

20160428 del

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Pin Strap Table - Pericom

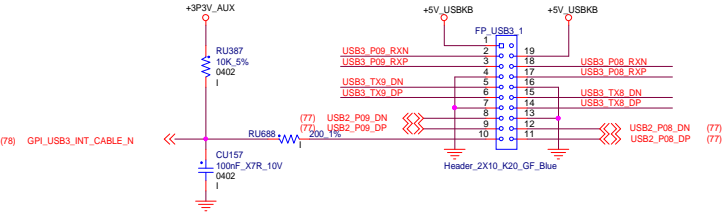
EQ_x	@2.5GHz	DE_x	
Pin#2	CHA	Pin#3	CHA
Pin#17	CHB	Pin#16	CHB
0	3dB	0	0dB
NC	6dB	NC	-3.5dB
1	9dB	1	-6dB



20160201 ESD component change to F10

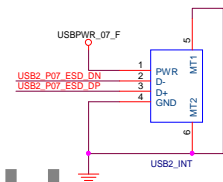
20161013 modify FP\_USB3\_1 material

AS POSSIBLE AS CLOSE

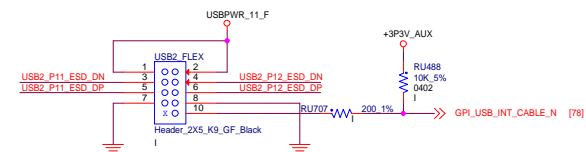
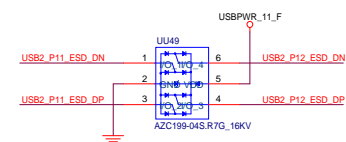




## INT USB2.0 Card Reader Header



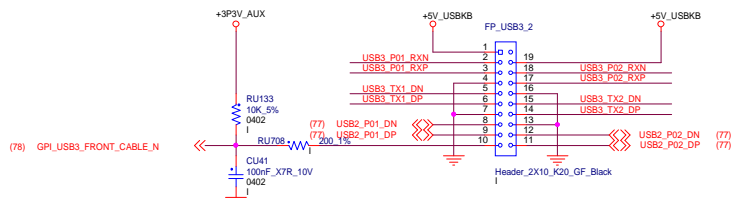
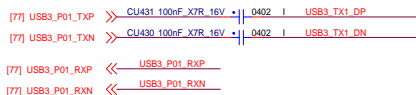
[www.aitech1.ru](http://www.aitech1.ru)



20160722 modify INT\_USB component

## INT USB3.0 Header

www.aitech1.ru

[illegible]

TITLE	INT USB 3.0
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DWG NO. MATIRA 5

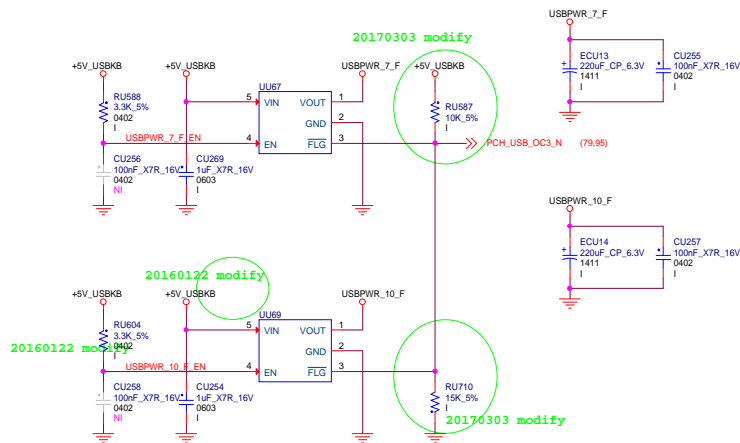
DATE Thursday, June 29, 2017

REV. X02

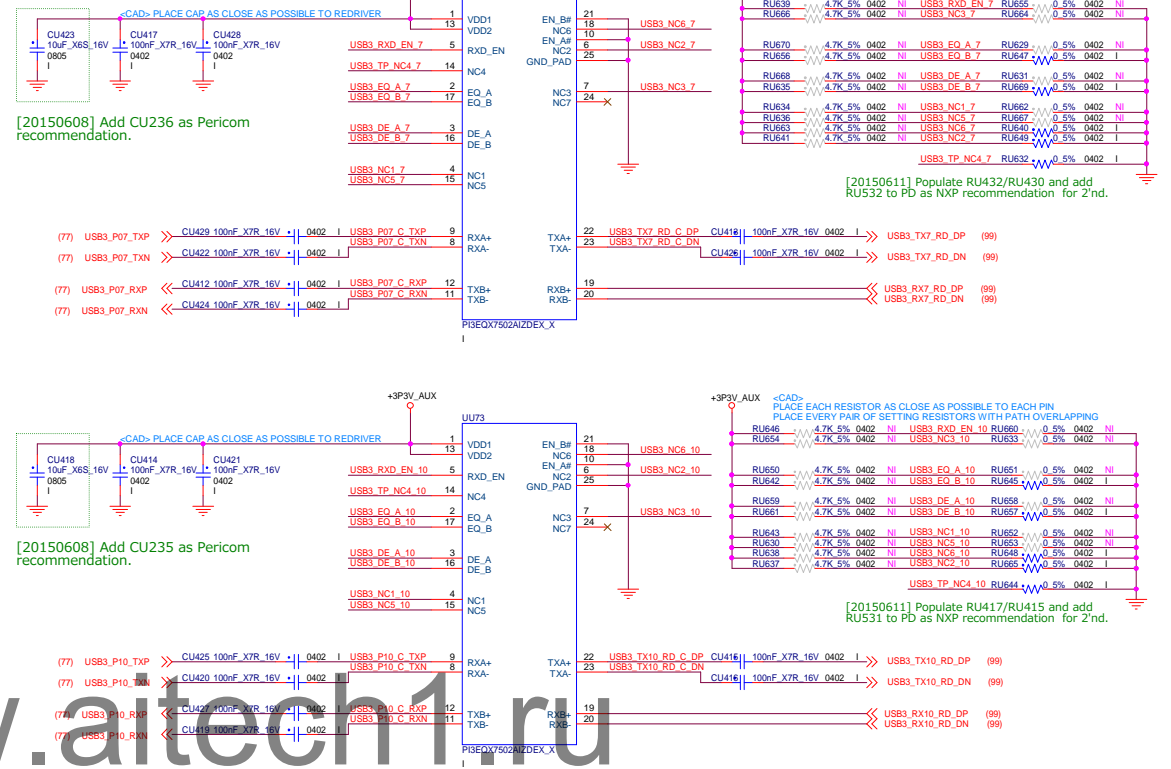
98 of 150

COMPRESSE  
IMAGE

# Rear USB3.0 Connector 20F2



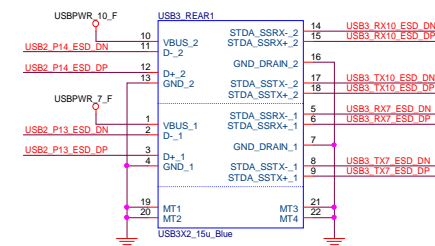
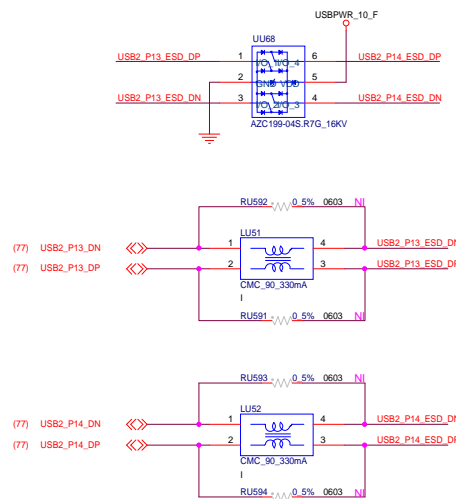
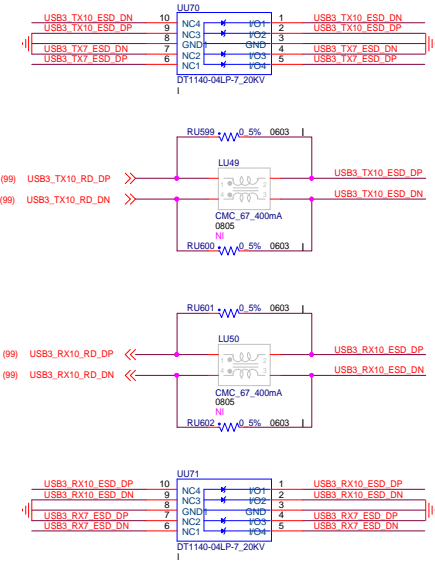
# USB3.0 REDRIVER



www.aitech1.ru


Pin Strap Table - Pericom

EQ_x	@2.5GHz	DE_x	
Pin#2	CHA	Pin#3	CHA
Pin#17	CHB	Pin#16	CHB
0	3dB	0	0dB
NC	6dB	NC	-3.5dB
1	9dB	1	-6dB

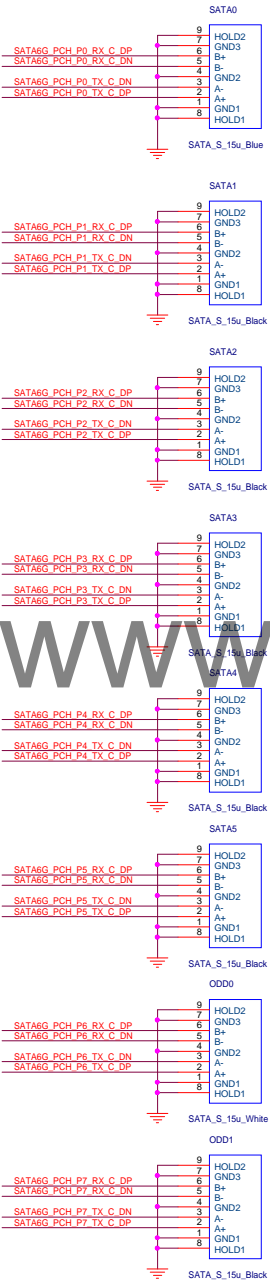
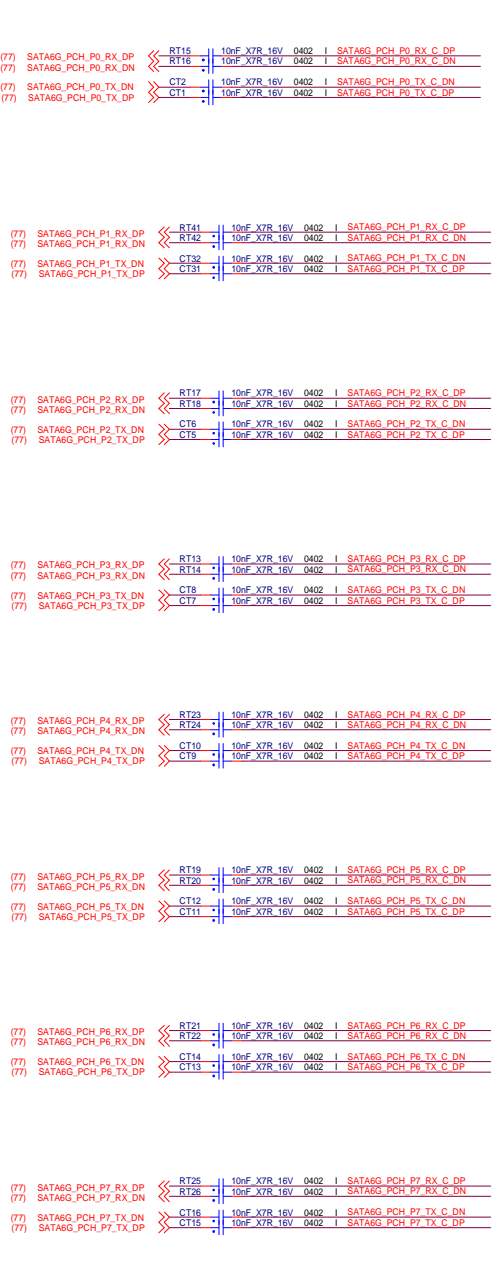


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	DWG NO. MATIRA 5		REV. X02	
	DATE Thursday, June 29, 2017		SHEET 100 of 150	

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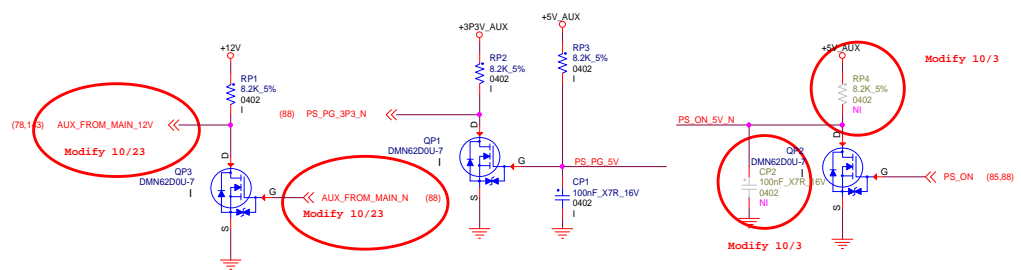
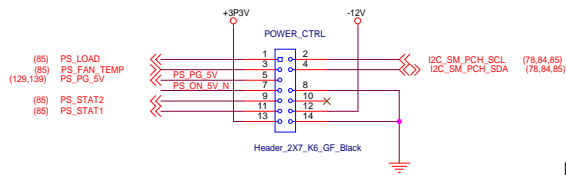
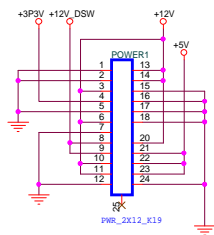
SATA Connector



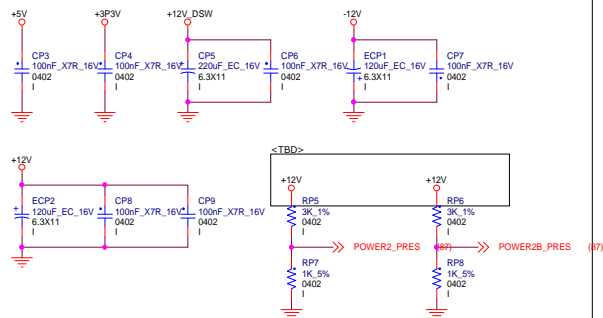
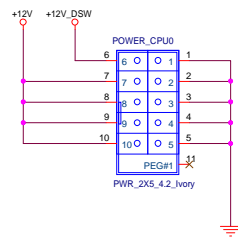
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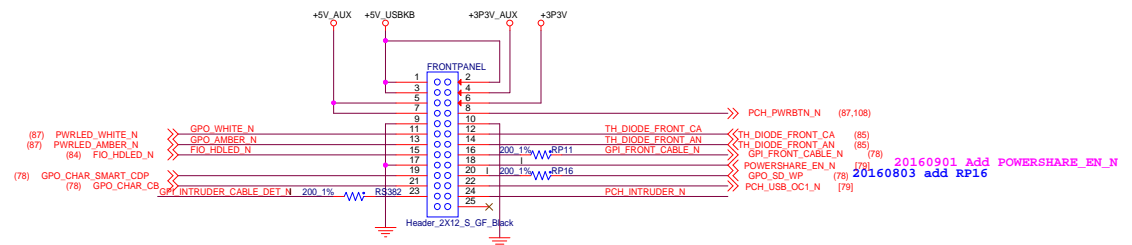
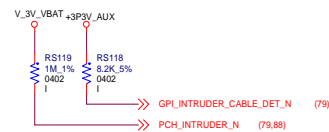
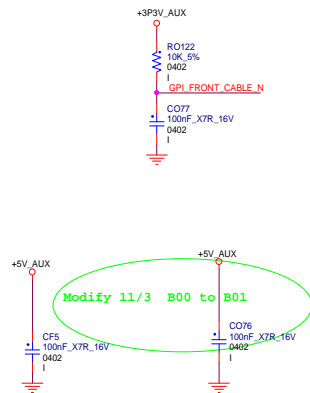
## POWER1 Connector



## POWER Switch



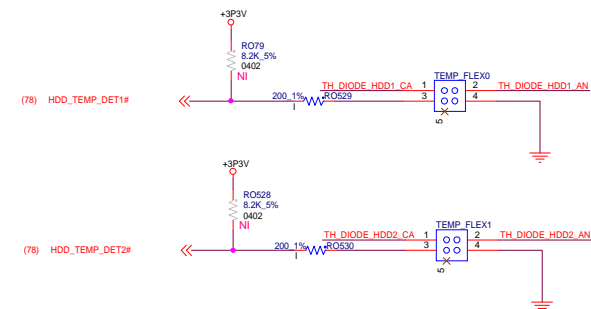
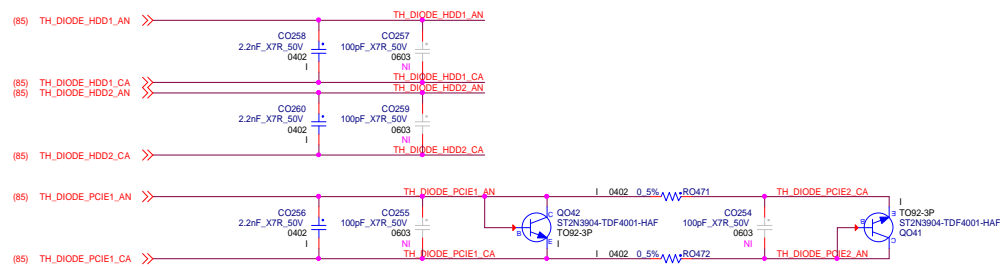
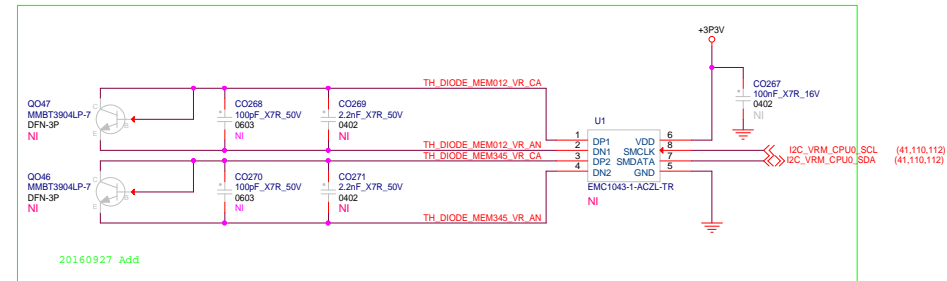
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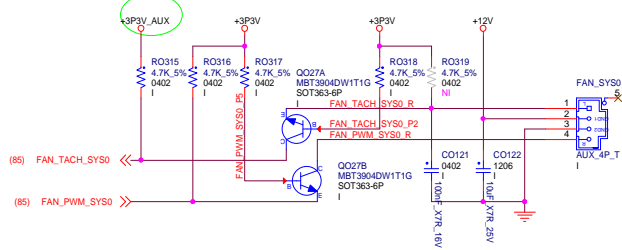
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<b>DWG NO.</b> MATRISA 5		<b>REV.</b> X02	
<b>DATE</b> Thursday, June 29, 2017		<b>SHEET</b> 104 of 150	



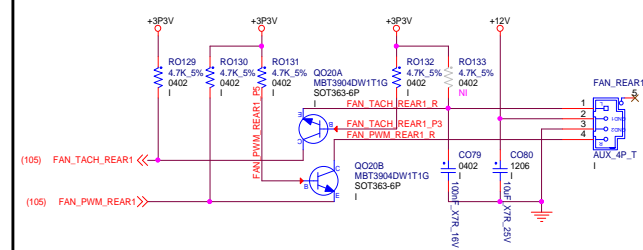
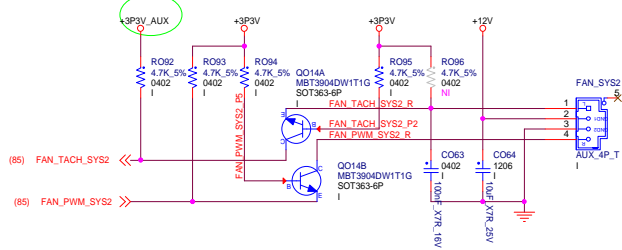
[www.aitech1.ru](http://www.aitech1.ru)



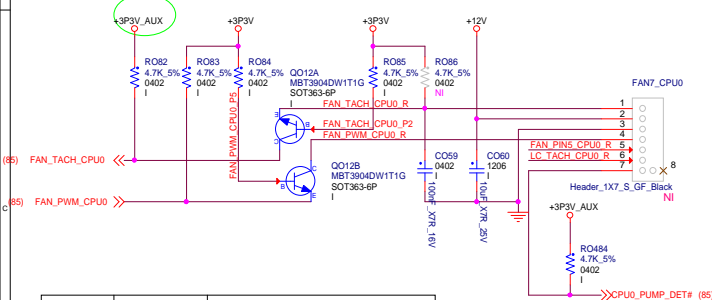
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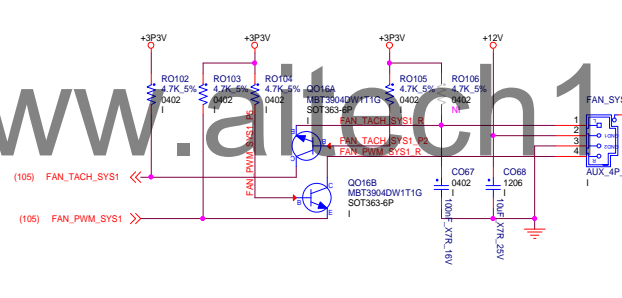
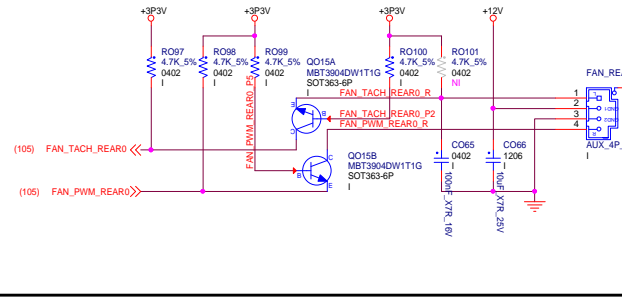
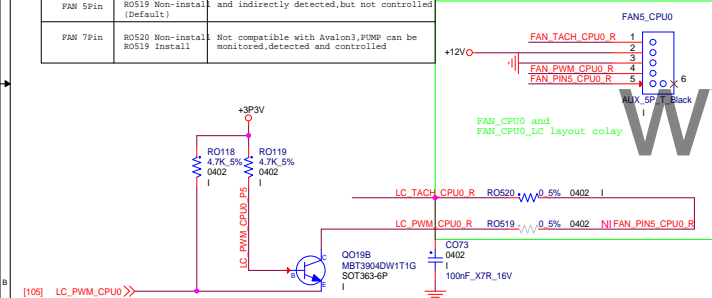
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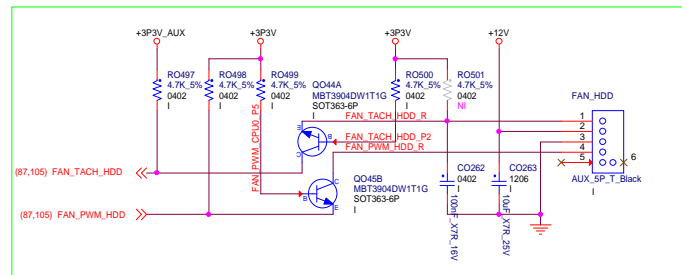
## 20160323 modify



FAN 5Pin	RO520 Install	Compatible with Avalon3,PUMP can be monitored and indirectly detected,but not controlled (Default)
FAN 7Pin	RO519 Non-install	
	RO520 Non-install	Not compatible with Avalon3,PUMP can be monitored,detected and controlled
	RO519 Install	



## 20160725 Add



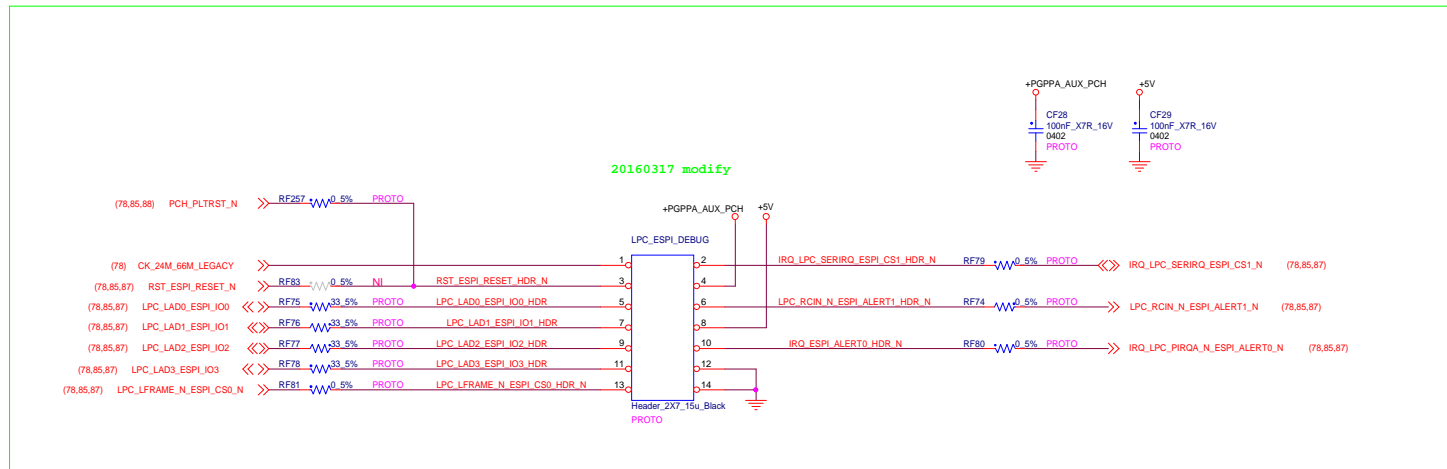
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TITLE: Fan Connector  
 DWG NO.: MATBIRA 5  
 DATE: Thursday, June 29, 2017  
 REV: X02  
 SHEET: 106 of 150

COMPRESSED IMAGE



## LPC/ESPI DEBUG HEADER

**Licence Label**

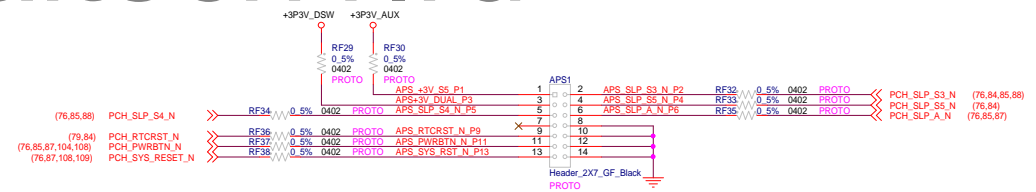
Note:  
AMI uEFI

20170316 modify

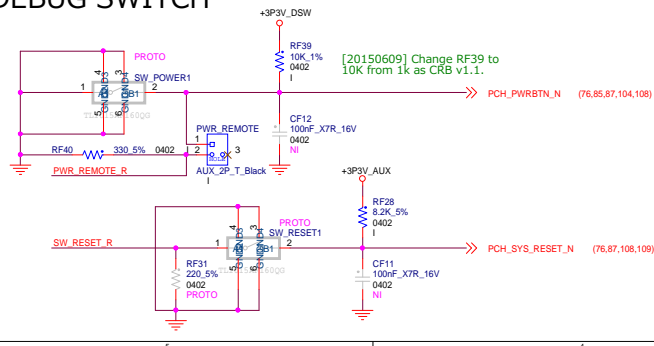
20170327 Remove BIOS\_LABEL

20170405 Add BIOS\_LABEL for BPM cost price

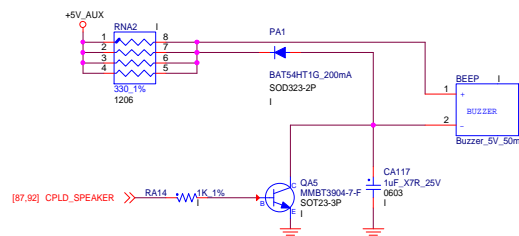
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## DEBUG SWITCH



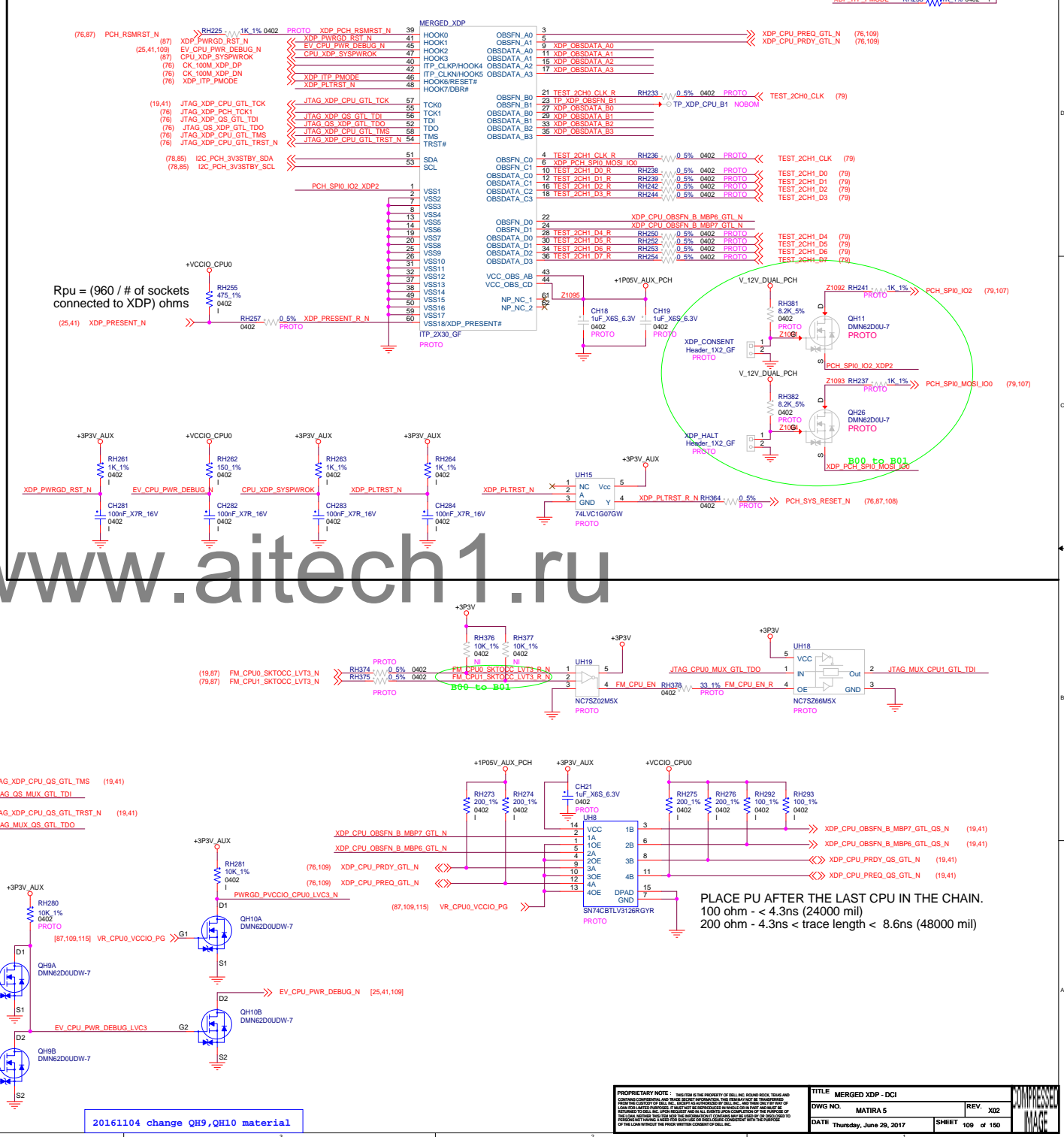
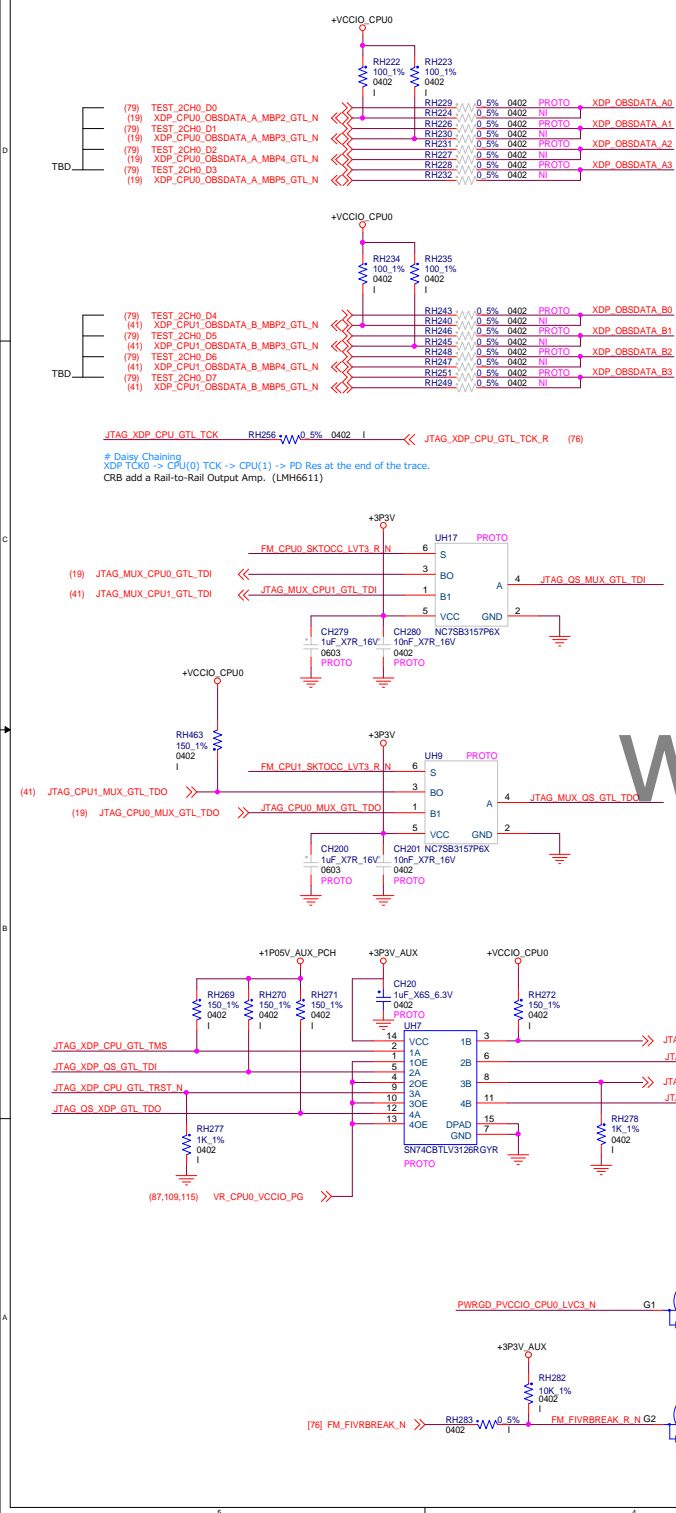
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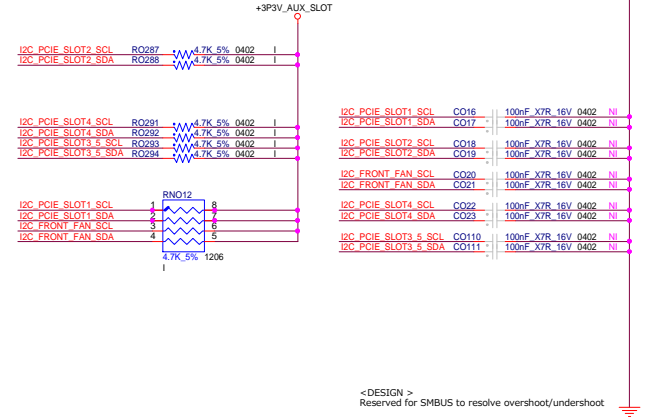
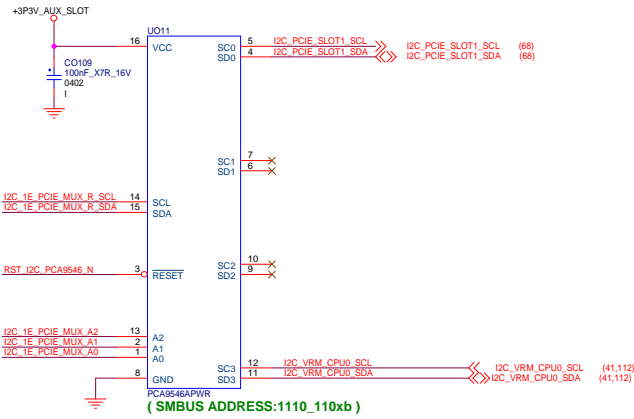
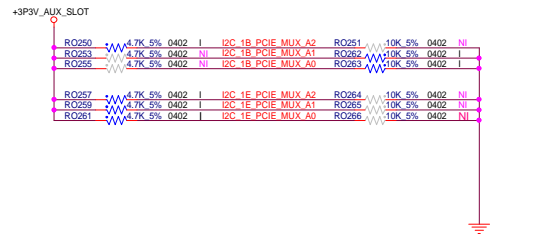
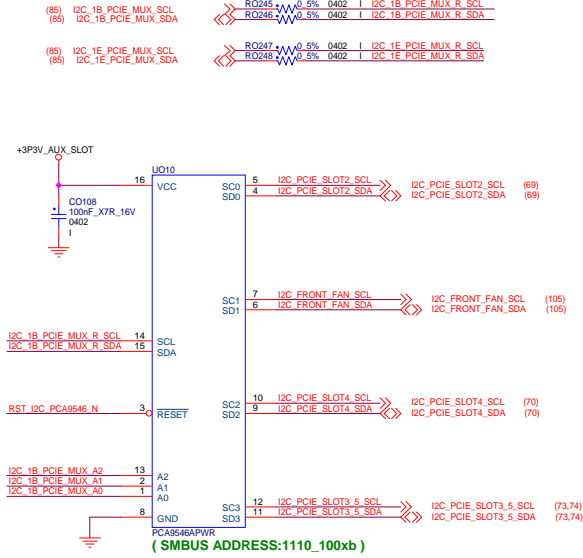
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TITLE		Debug/Label/Misc	
DWG NO.		MATIRA 5	REV. X02
DATE		Thursday, June 29, 2017	SHEET 108 of 150

## MERGED XDP - DCI

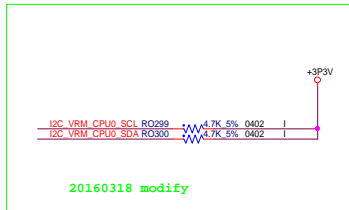
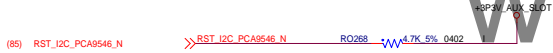


## SMBUS MUX



<DESIGN >  
Reserved for SMBUS to resolve overshoot/undershoot

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# COMPRESSED IMAGE

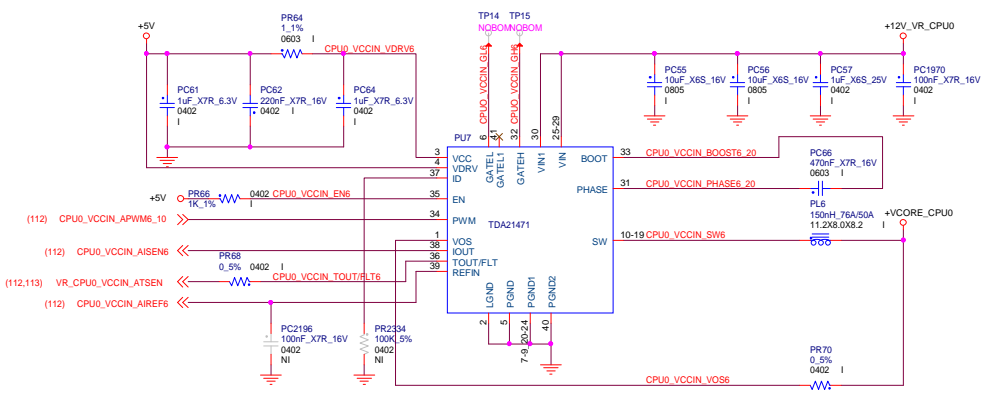
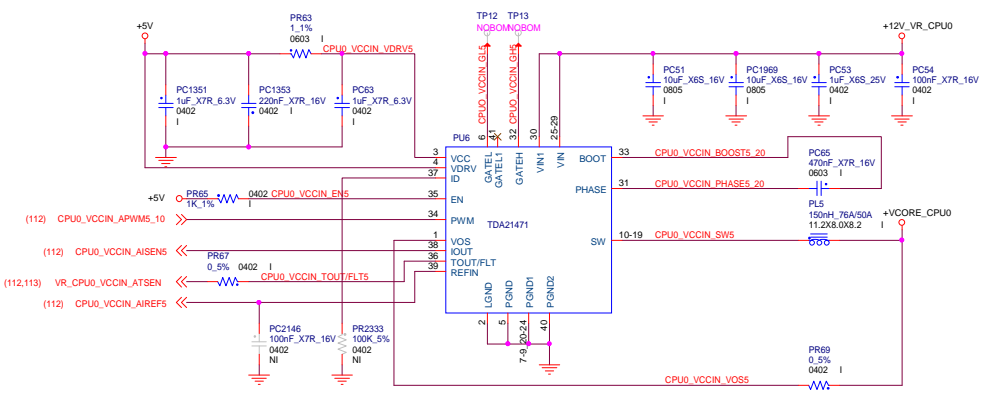
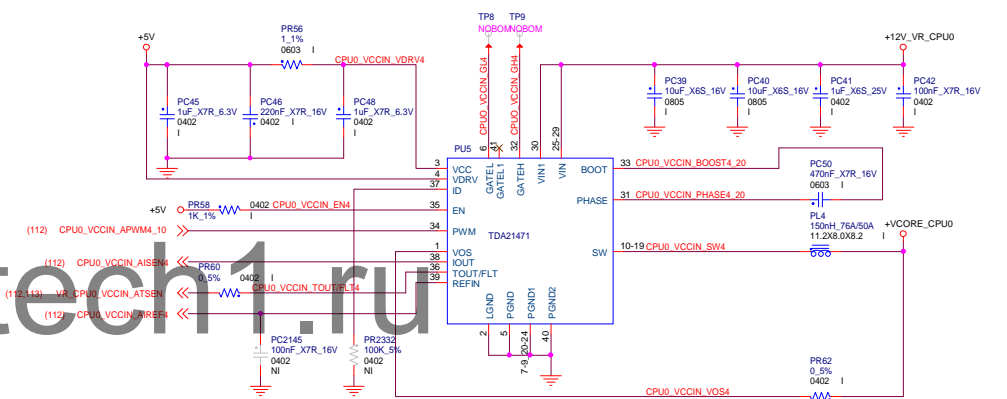
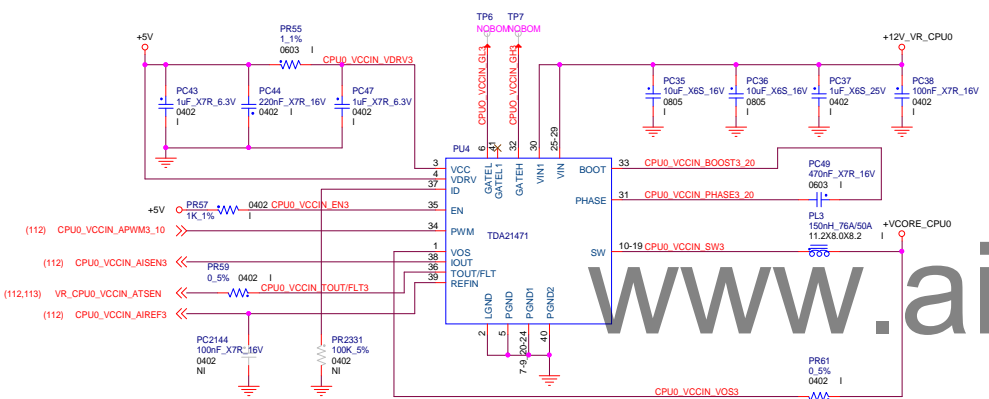
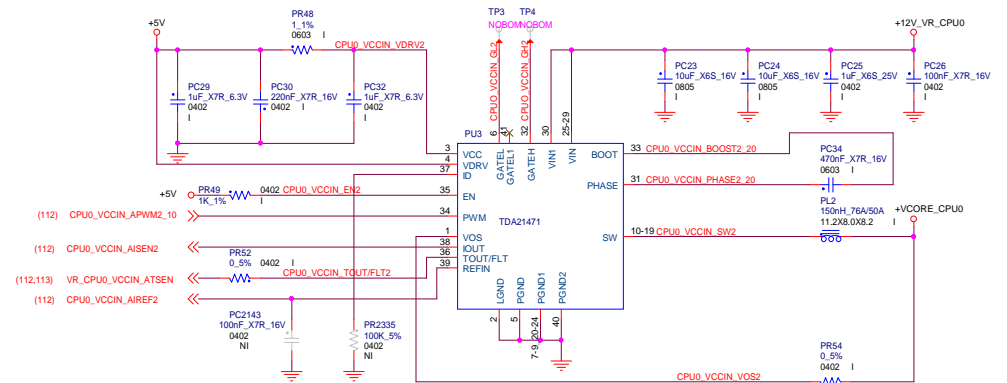
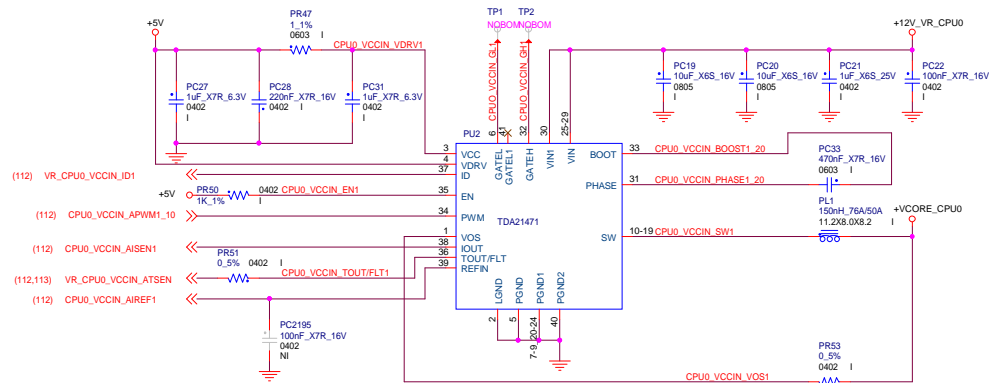


```
VCCIN/SA SVID Address:0,1
PMBus Address:0xC0
```

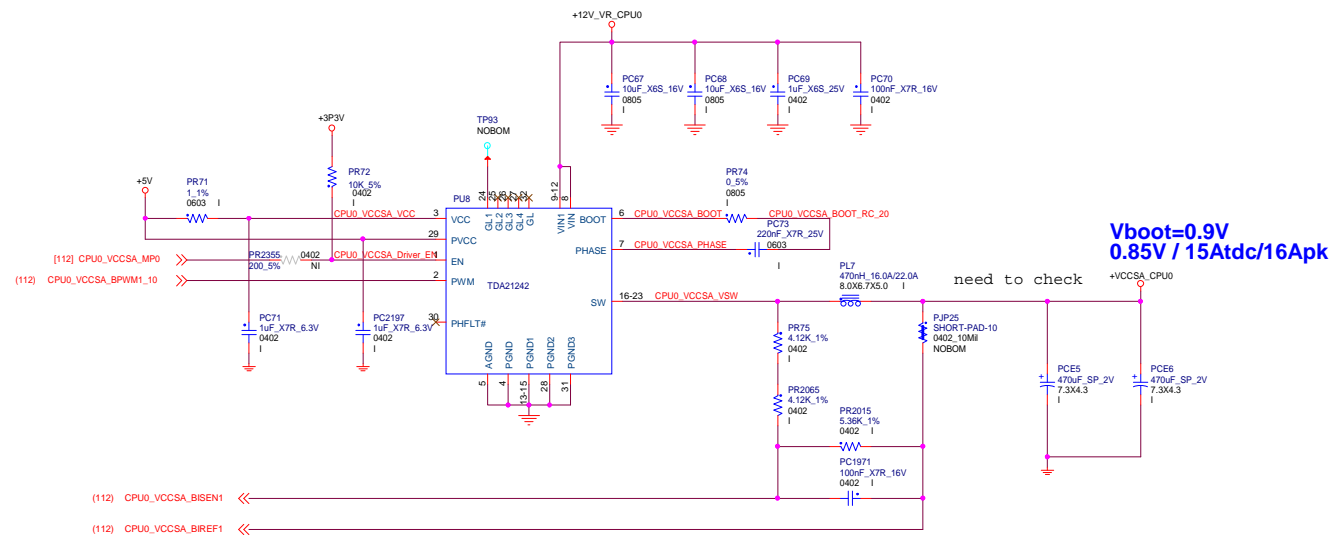
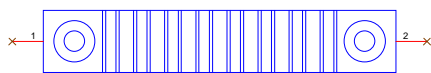




## +VCORE\_CPU0\_Driver



VR\_HEATSINK\_CPU0  
HEATSINK\_VR Mosfet  
76.6X8.2X20.0 I



**CPU0 VCCIN CAP** +1.8V / 89Atdc/228Apk  
Vboot=1.7V

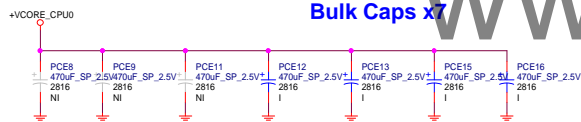
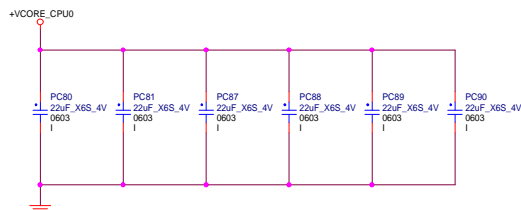
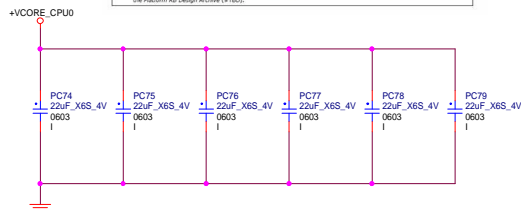


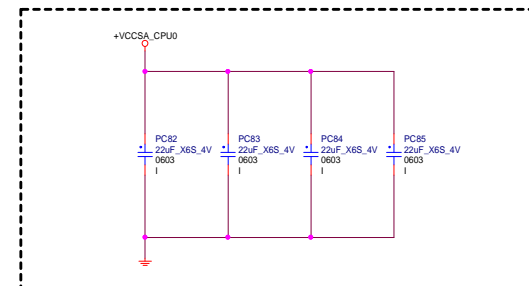
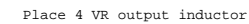
Table 204. CPU VccIN VR13.0 Recommended Output Caps per Socket, Based on Lightning Ridge RB Design

Cap Description	Min Quantity	Notes
470 $\mu$ F / 2.5V / 20% / Alum / 3018	7	Bulk caps, place close to VR1's output inductor's pads (2 top layer, 5 bottom layer)
22 $\mu$ F / 4V / 20% / MSL / 0605	12	place close to the inductor pad (4 top layer, 8 bottom layer)
10 $\mu$ F / 6.3V / 20% / Alum / 0603	40	place in the socket cavity (bottom layer)
10 $\mu$ F / 6.3V / 20% / Alum / 0603	45	place in the socket cavity (top layer)

**Note:** The above decoupling caps are Min recommended for our VR13.0 design used in the RBS. But each designer should review their chosen VR topology and adjust the required caps accordingly for up to and including 13M step load frequency. Intel package decoupling has been selected to address frequencies above 1Mhz. For additional details, see [Intel VR Design guide \(PDF\)](#).



**CPU0 VCCSA CAP**



**Table 211. PVCCSA VR Bulk / Decoupling Caps Based on Neon City RB**

Cap Value	Min Quantity per VR	Notes
470 $\mu$ F / 2.5V / 20% / Alum / 3018	2	bulk, place close to VR output inductor (Top layer)
22.0 $\mu$ F / 4V / 10% / X6S / 0805	5	place 2 VR output inductor (Top layer) and 3 at socket cavity (Bottom layer)
10.0 $\mu$ F / 6.3V / 10% / X6S / 0603	4	place all at Top Layer at socket cavity

```
CPU0
VCCIO SVID Bus= 02h
```



## +VCCIO\_CPU0\_DRIVER

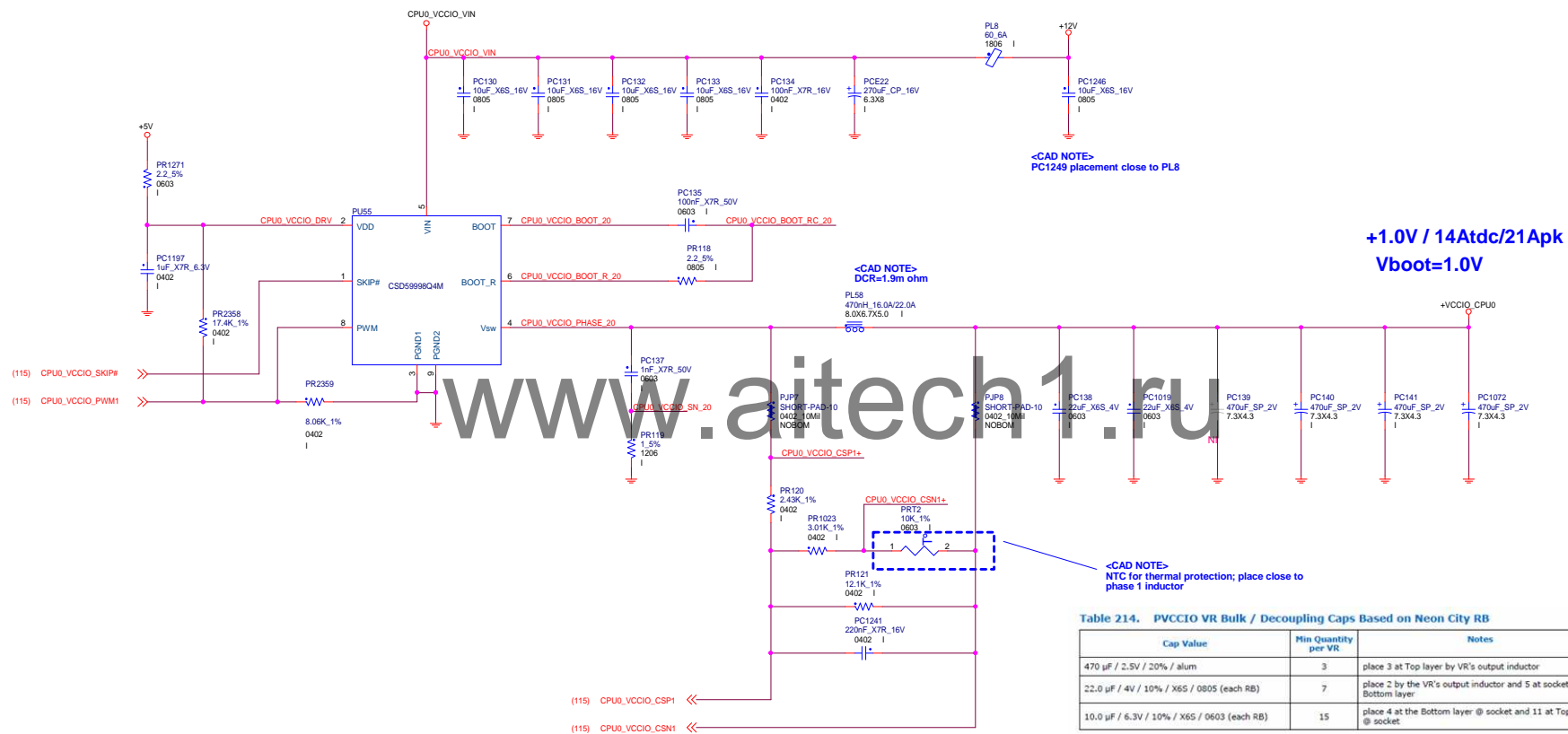


Table 214. PVCCIO VR Bulk / Decoupling Caps Based on Neon City RB

Cap Value	Min Quantity per VR	Notes
470 $\mu$ F / 2.5V / 20% / alum	3	place 3 at Top layer by VR's output inductor
22.0 $\mu$ F / 4V / 10% / X6S / 0805 (each RB)	7	place 2 by the VR's output inductor and 5 at socket cavity Bottom layer
10.0 $\mu$ F / 6.3V / 10% / X6S / 0603 (each RB)	15	place 4 at the Bottom layer @ socket and 11 at Top layer @ socket

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TITLE	VR, CPU0 VCCIO DRIVER
DWG NO.	MATIRA 5
DATE	Thursday, June 29, 2017

COMPRESSED  
IMAGE


[illegible]

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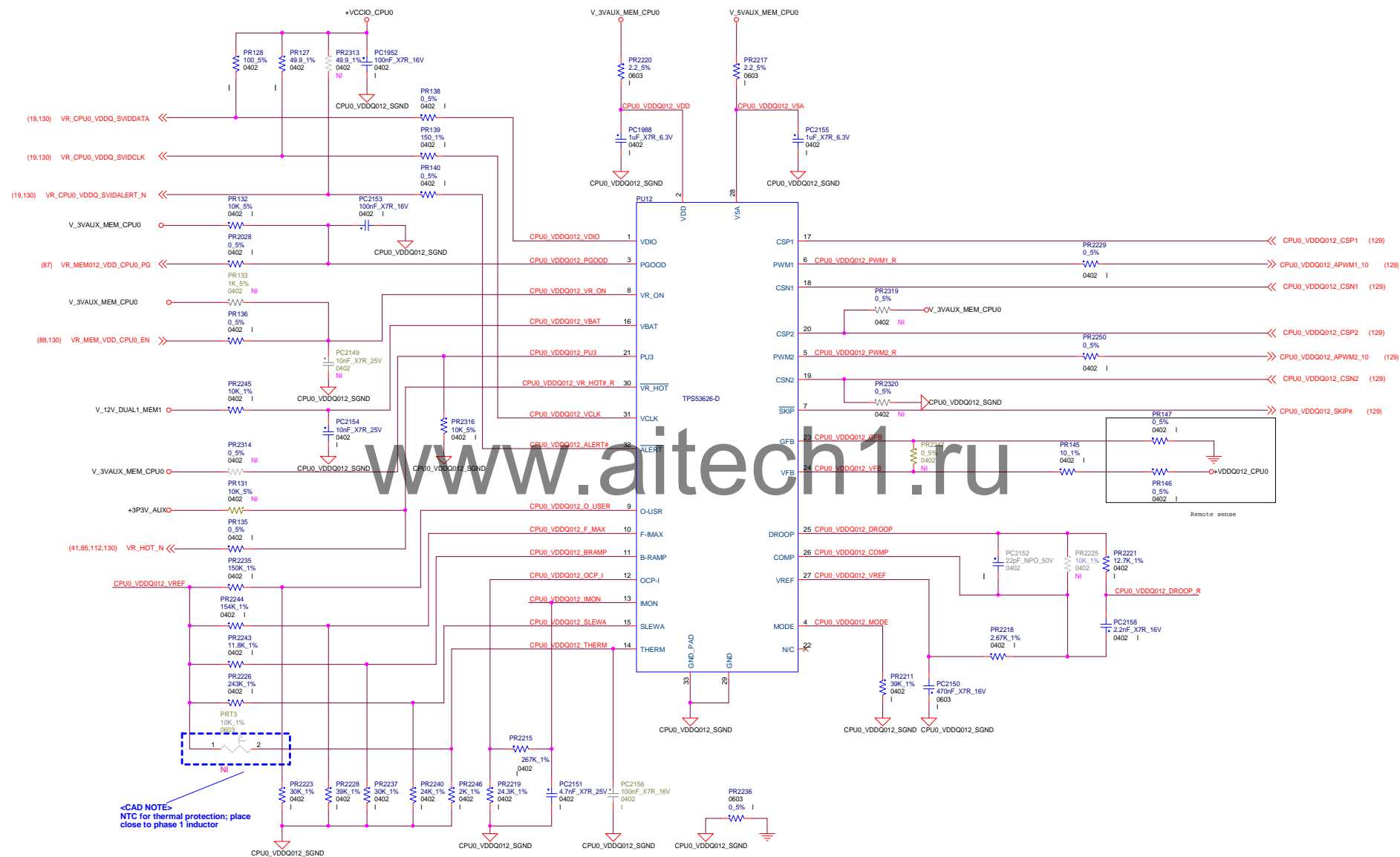
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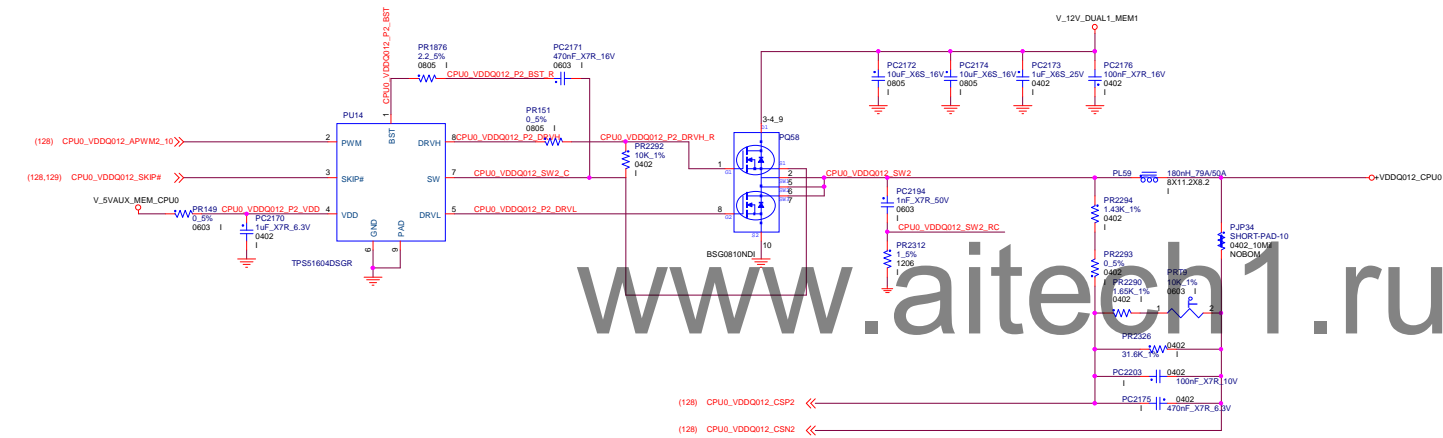
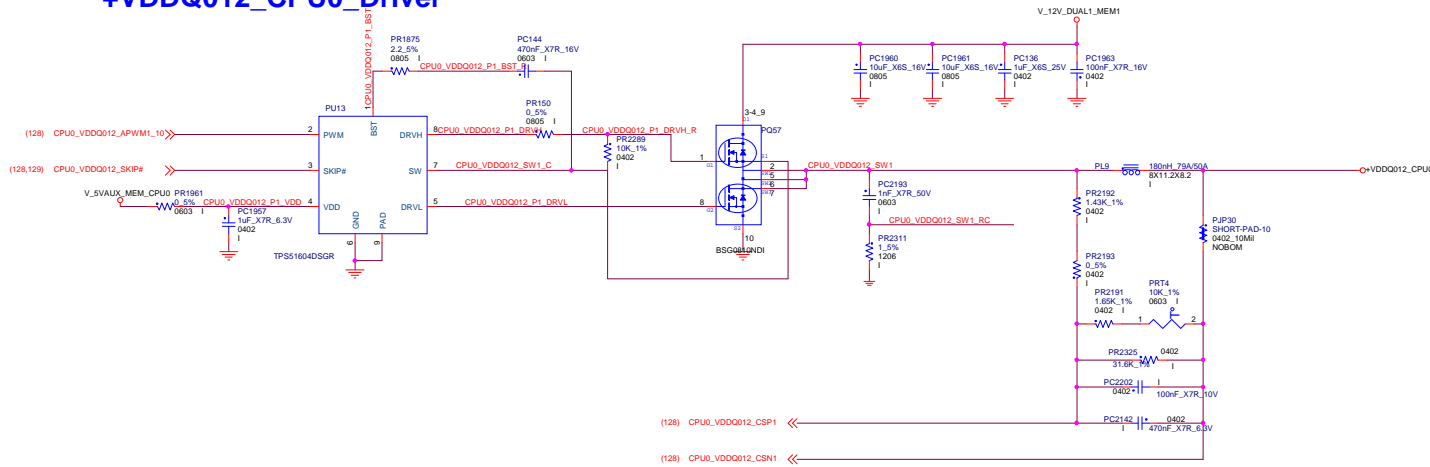
[illegible]

# +VDDQ012\_CPU0\_Controller





# +VDDQ012\_CPU0\_Driver



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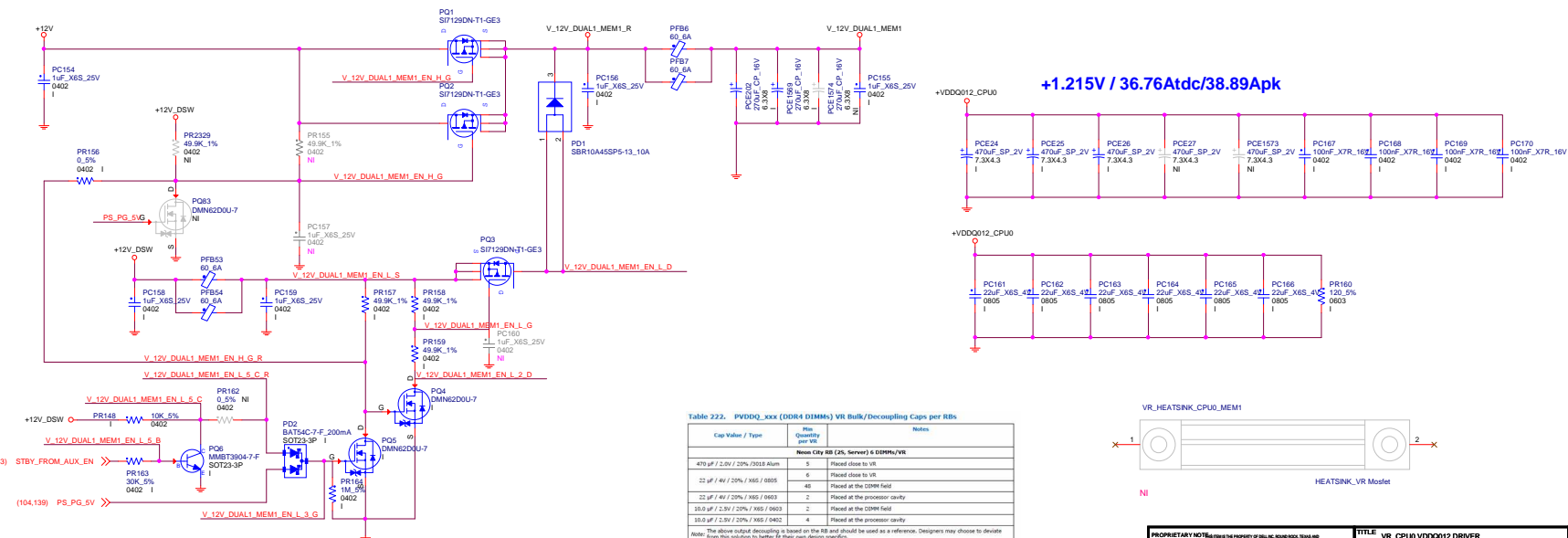
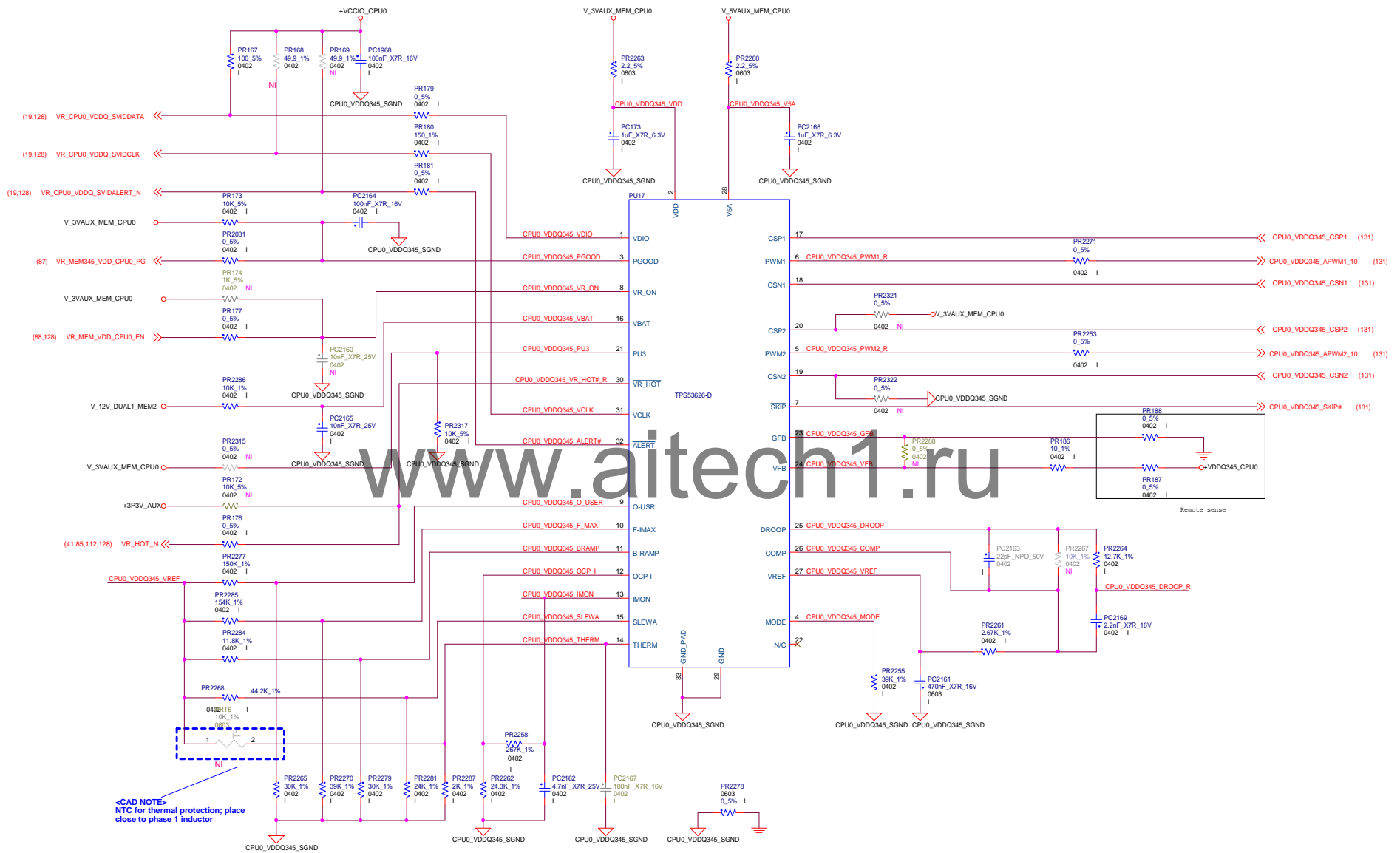


Table 222. +VDDQ012\_CPU0 (DDR4 DIMMs) VR Bulk/Decoupling Caps per RBS

Cap Value / Type	Qty	Quantity per VR	Notes
Neon City 88 (2% Server) & G38H/VR			
470 µF / 2.0V / 20% / 3018 Alum	5	Placed close to VR	
22 µF / 4V / 20% / X65 / 0805	6	Placed close to VR	
	40	Placed at the DIMM field	
22 µF / 4V / 20% / X65 / 0603	2	Placed at the processor cavity	
10.0 µF / 2.5V / 20% / X65 / 0603	2	Placed at the DIMM field	
10.0 µF / 2.5V / 20% / X65 / 0402	4	Placed at the processor cavity	
The above output decoupling is based on the RB and should be used as a reference. Designers may choose to deviate from this solution to better fit their own design specifics.			



## +VDDQ345\_CPU0\_Controller



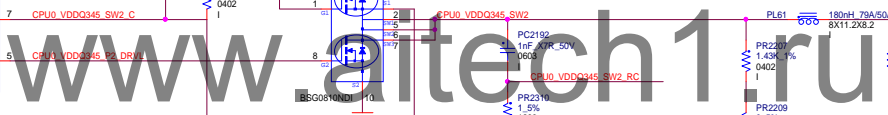
<CAD NOTE>  
NTC for thermal protection; place  
close to phase 1 inductor

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TITLE	VR, CPU0 VDDQ345 CONTROLLER	
DWG NO.	MATIRA 5	
DATE	Thursday, June 29, 2017	SHE

COMPRESSED  
IMAGE

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**Note:** The above output decoupling is based on the RB and should be used as a reference. Designers may choose to deviate from this solution to better fit their own design specifics.



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	<p><b>DATE</b> Thursday, June 29, 2017</p>	<p><b>SHEET</b> 135</p>	<p><b>OF THE</b> 150</p>

## CPU0 MEM VPP

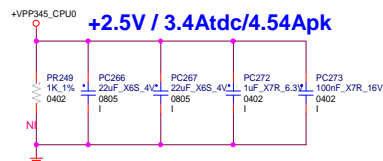
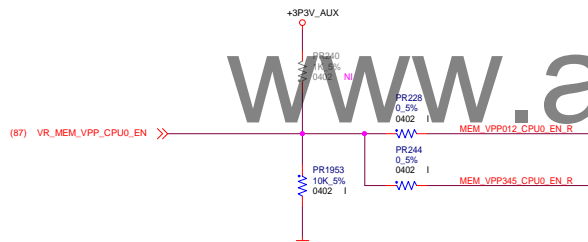
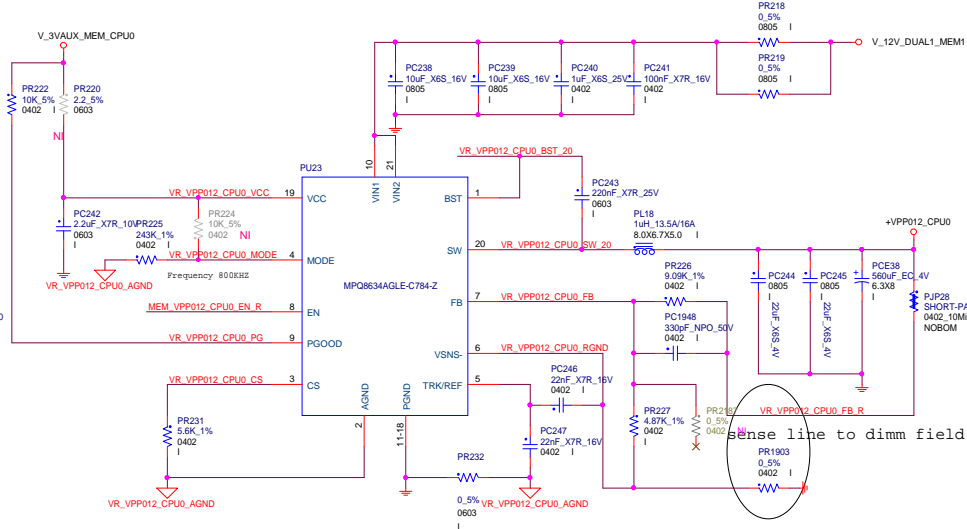
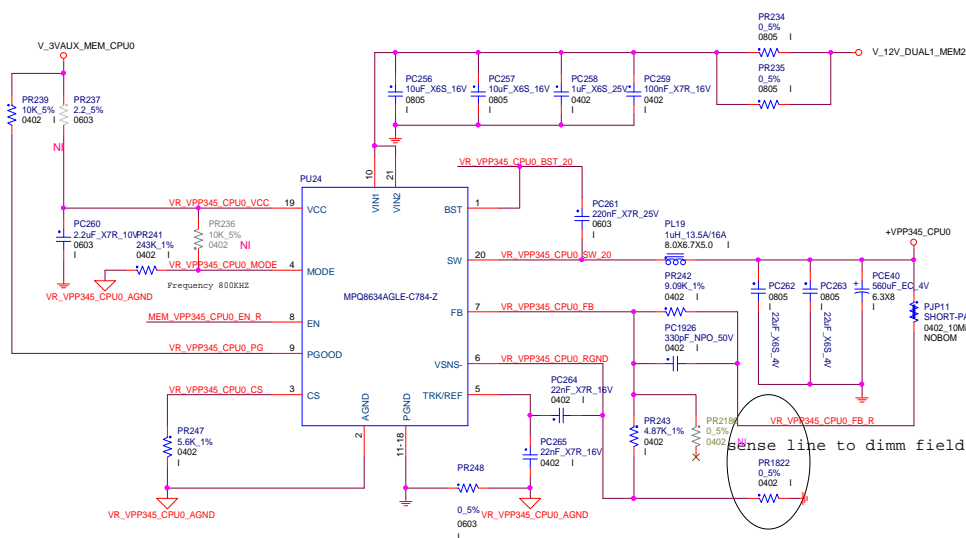


Table 227. PVPP\_XXX VR Bulk / Decoupling Caps, per Neon City RB

Cap Value	Min Quantity per VR	Notes
<b>RD ( 2% Server) 6.DIMMs / VR</b>		
560 $\mu$ F / 4V / 10% / Alum THMT		Bulk, place close to VR output inductor
Cap Value	Min Quantity per VR	Notes
22.0 $\mu$ F / 4V / 20% / X6S / 0605	6	Place 2 close to VR output inductor (bottom), 4 between DIMMs (top)
10.0 $\mu$ F / 4V / 20% / X6S / 0603	8	Place between DIMMs, 2 caps/DIMM

Note: The above output decoupling is based on the RfE and should be used as a reference. Designers may choose to deviate from these values.

Note: The above output decoupling is based on the RBs and should be used as a reference. Designers may choose to deviate from this solution to better fit their design specifics.

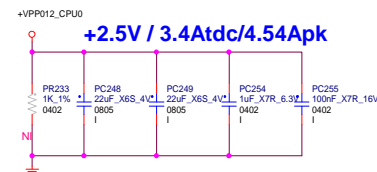


Table 227. PVPP\_xxx VR Bulk / Decoupling Caps, per Neon City RB

Cap Value	Pin Quantity per VR	Notes
<b>RD (2), SerVO, 6 DIPMs / VR</b>		
560 $\mu$ F / 4V / 10% / Alum THHT	3	Bulk, place close to VR output inductor
Cap Value	Pin Quantity per VR	Notes
22.0 $\mu$ F / 4V / 20% / M6505 / 0805	6	Place 2 close to VR output inductor (bottom), 4 between DIPMs
10.0 $\mu$ F / 4V / 20% / M655 / 0603	8	Place between DIPMs, 2 caps/DIPM

Note: The above output decoupling is based on the RRs and should be used as a reference. Designers may choose to deviate from the above design to meet their own needs.

Note: The above output decoupling is based on the RBs and should be used as a reference. Designers may choose to deviate from this solution to better fit their design specifics.



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## DDR\_VTT

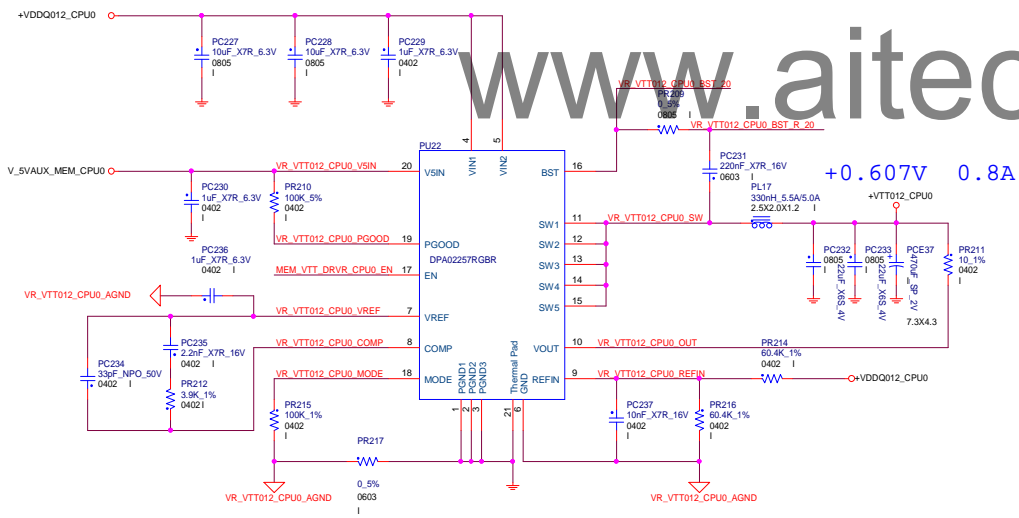
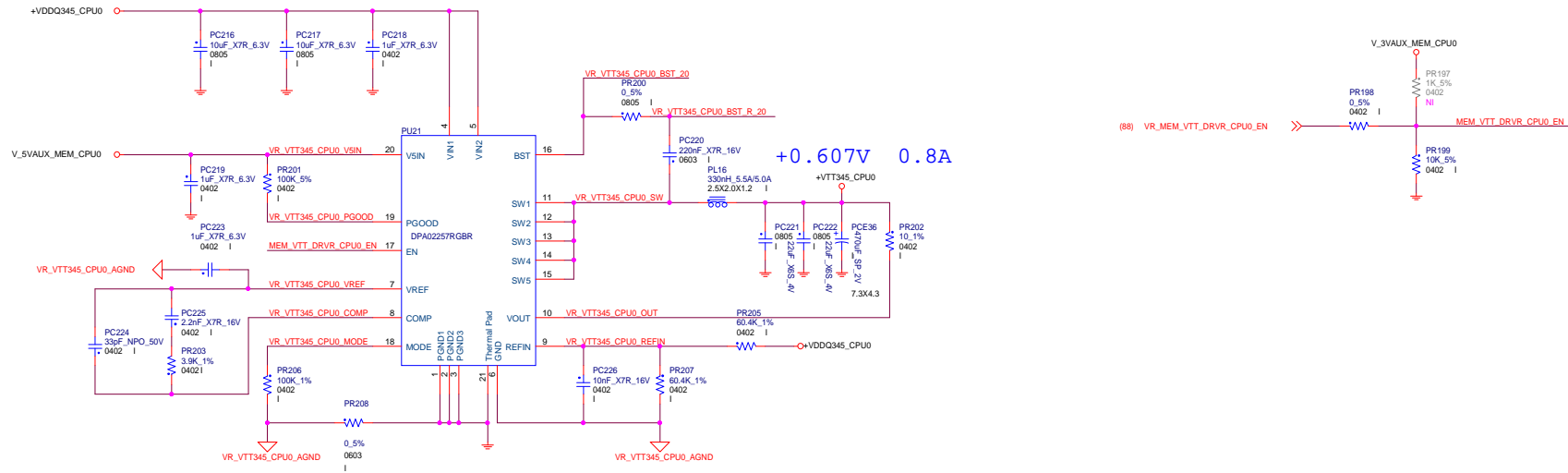


Table 225. PVTT\_xxx VR (DDR4) Bulk/Decoupling Caps per RBs

Cap Value/ Type	Max Quantity per VR	Notes
<b>Neon City RB (25, Server) 6 DIMMs / VR</b>		
47 $\mu$ F / 2.5V / 20% / X65 / 0805	3	at VTT DIMM pin field
470 $\mu$ F / 2.0V / 20% / Alum	1	Place close to VR output
22 $\mu$ F (Al.OV) / 20% / X65 / 0805	1	
22 $\mu$ F (Al.OV) / 20% / X58 / 0805	3	at VTT DIMM pin field

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TITLE	VR. MEMORY VTT
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DWG NO.	MATIBA E
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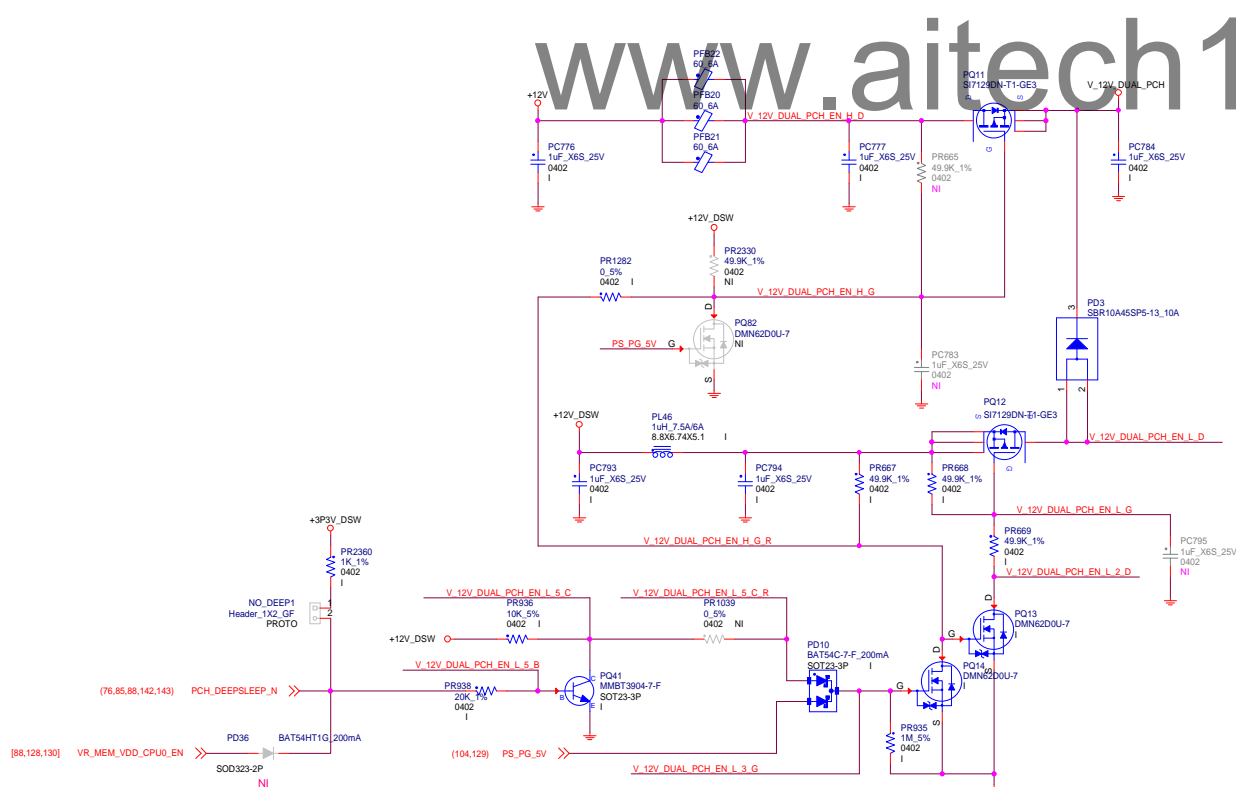
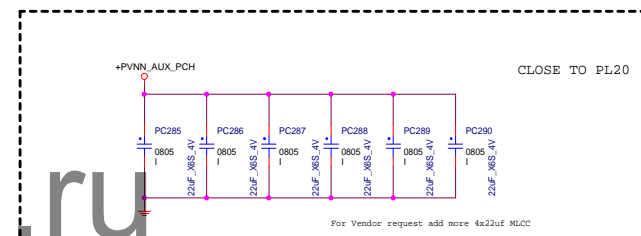
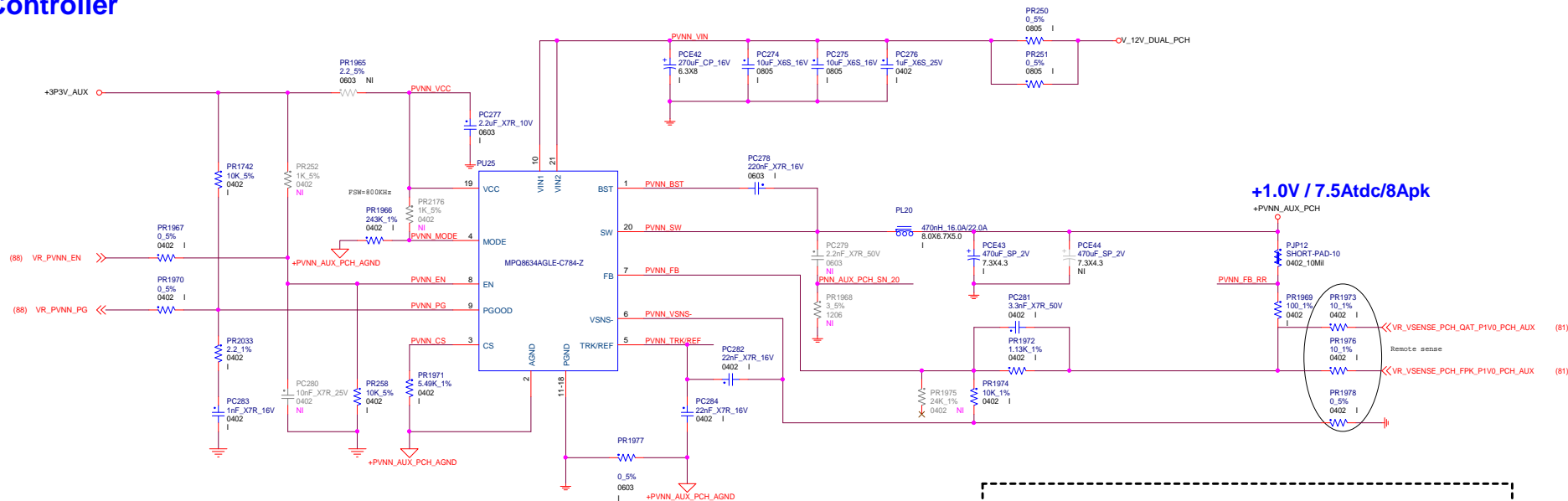
DATE Thursday, June 29, 2017

REV. 400

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COMPRESSED  
IMAGE

## +VNN\_Controller



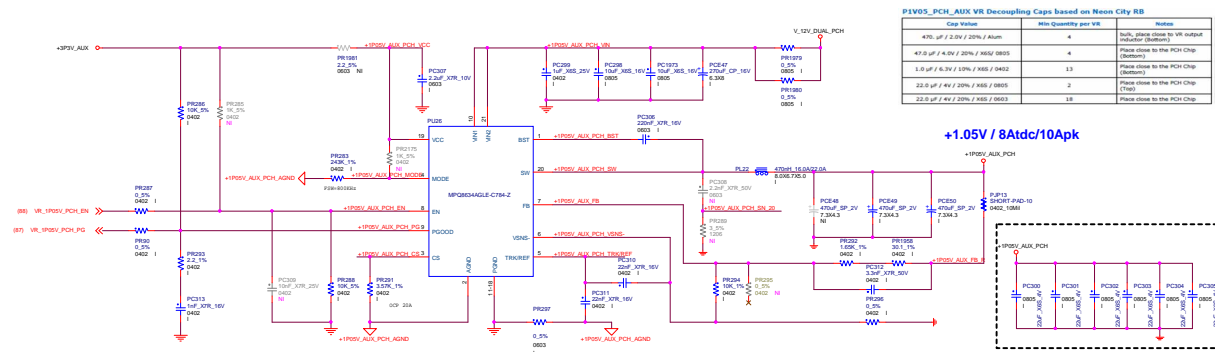
PVNN\_PCH\_AUX VR Decoupling Caps based on Neon City RB

Cap Value	Min Quantity per VR	Notes
470 $\mu$ F / 2.0V / 20% / AlPoly	3	bulk, place close to VR output inductor
47.0 $\mu$ F / 4.0V / 20% / X6S / 0805	4	Place close to the PCH chip (bottom)
1.0 $\mu$ F / 6.3V / 10% / X6S / 0402	18	Place close to the PCH
22.0 $\mu$ F / 4.0V / 20% / X6S / 0603	18	Place close to the PCH (bottom)
22.0 $\mu$ F / 4.0V / 20% / X6S / 0805	2	Place close to the VR Output Inductor (bottom)

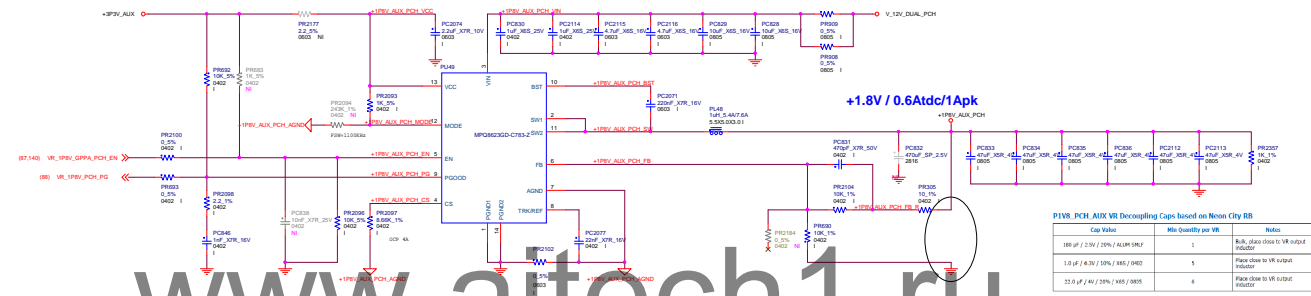
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TITLE VR. PVNN CONTROLLER		COMPRESSED IMAGE
DWG NO. MATIRA 5	REV. A00	
DATE Thursday, June 29, 2017	SHEET 139 of 150	

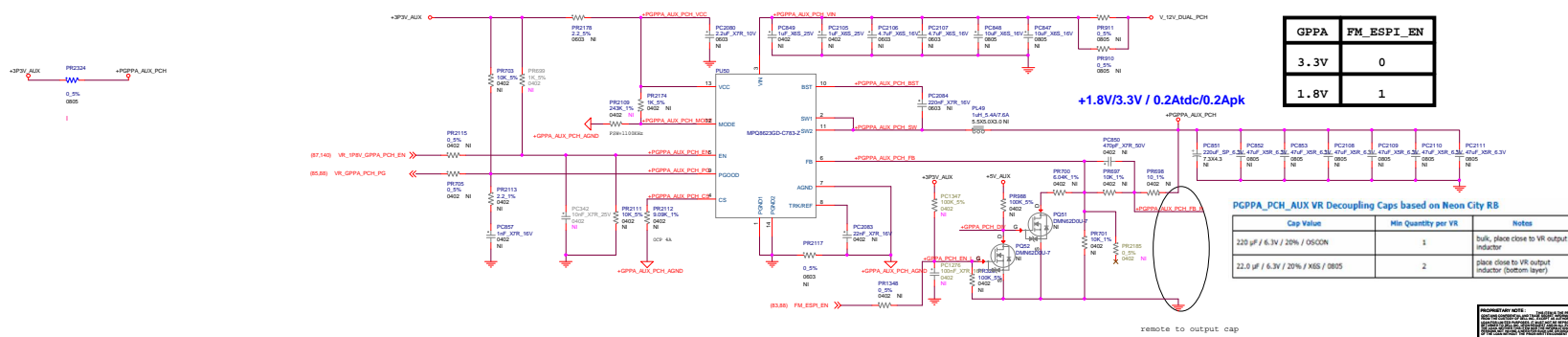
+1P05V\_AUX\_PCH\_Controller





+1P8V\_Controller




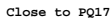
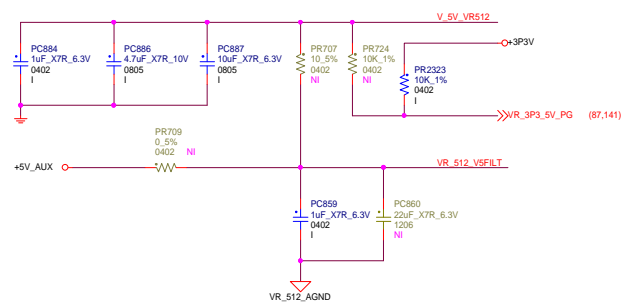
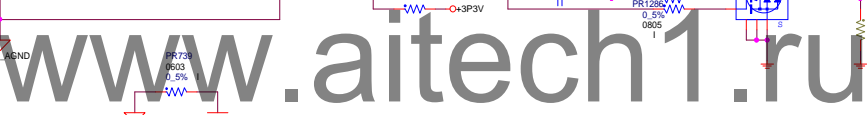
+PGPPA\_Controller



[41,142] VR\_+5V\_AUX\_PG >> 

(88) VR\_MAIN\_EN >> 

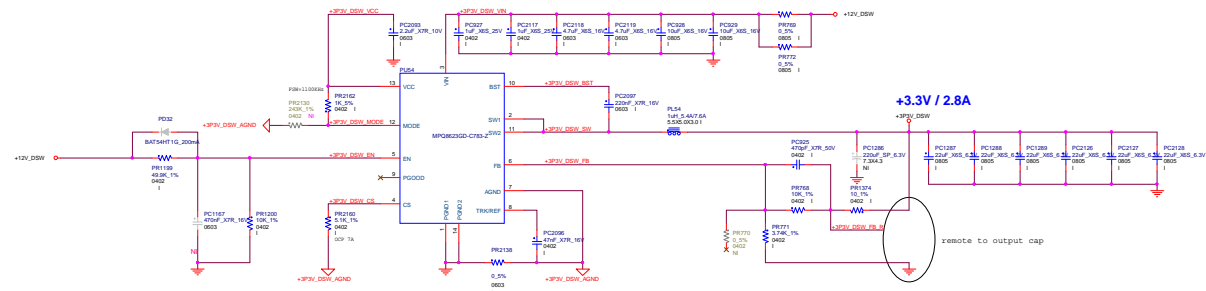
(87) VR\_3P3V\_EN >> 



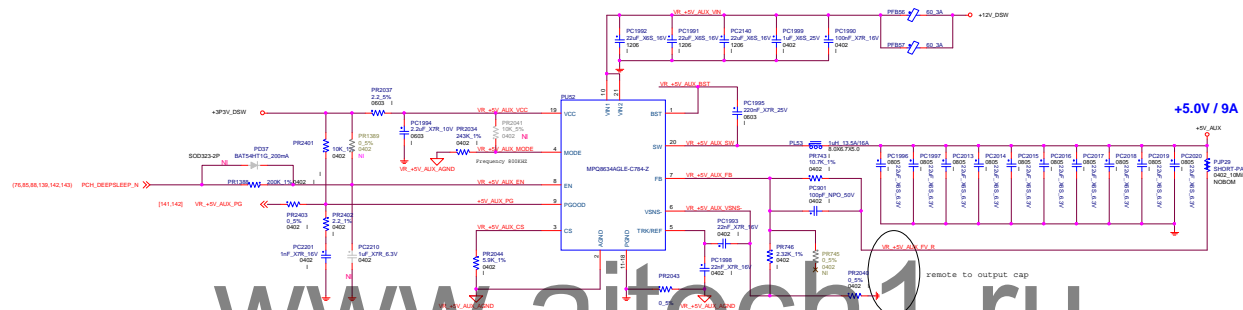
Close to PQ19

TITLE		VR. 5V , 3.3V	
DWG NO.		MATIRA 5	REV. A00
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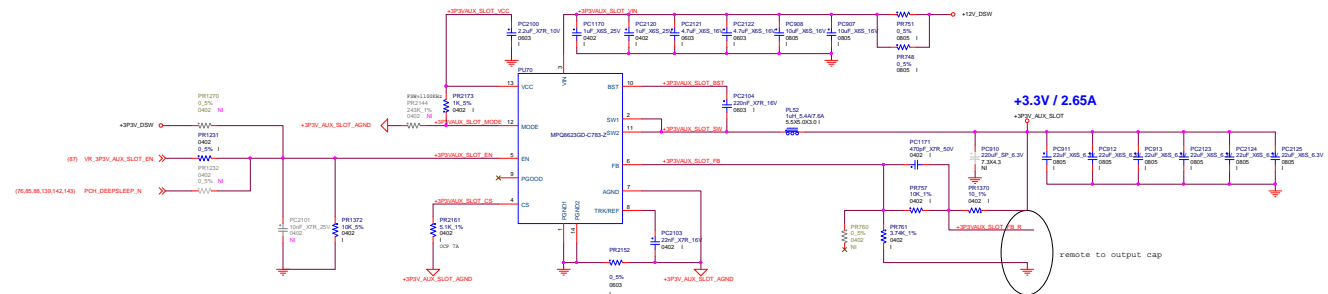
## +3P3V\_DSU



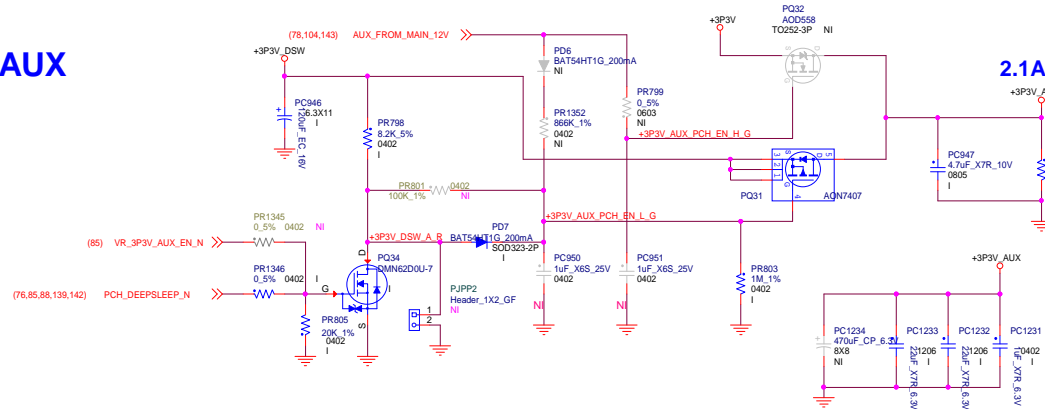
## +5V\_AUX



## +3P3V\_AUX\_SLOT

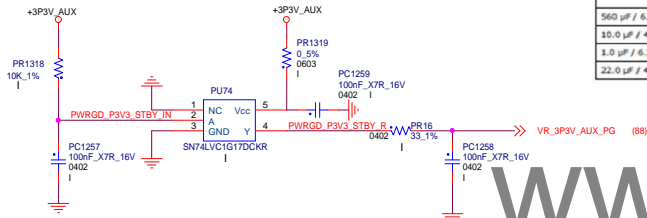


## +3P3V\_AUX



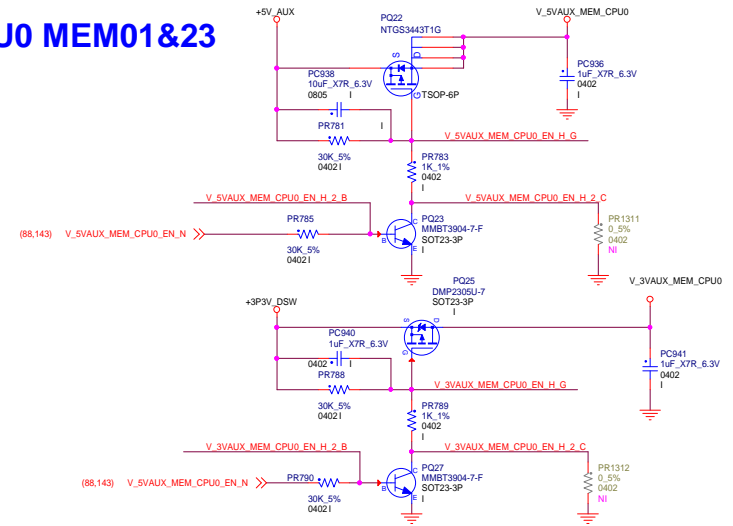
P3V3\_AUX VR Decoupling Caps based on Neon City RB

Cap Value	Min Quantity per VR	Notes
560 $\mu$ F / 6.3V / 20% / Alum	1	Bulk, place close to VR output inductor
10.0 $\mu$ F / 4.0V / 20% / X6S / 0603	6	
1.0 $\mu$ F / 6.3V / 10% / X6S / 0402	3	
22.0 $\mu$ F / 4.0V / 20% / X6S / 0805	2	Place close to VR output inductor

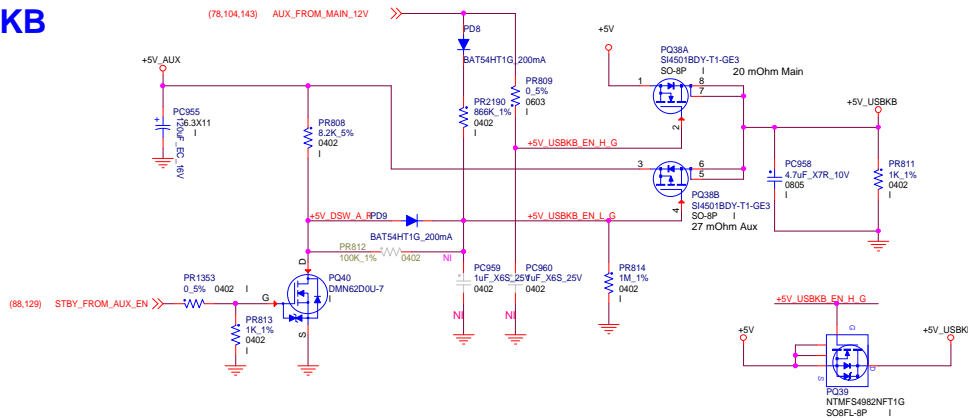


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## CPU0 MEM01&23



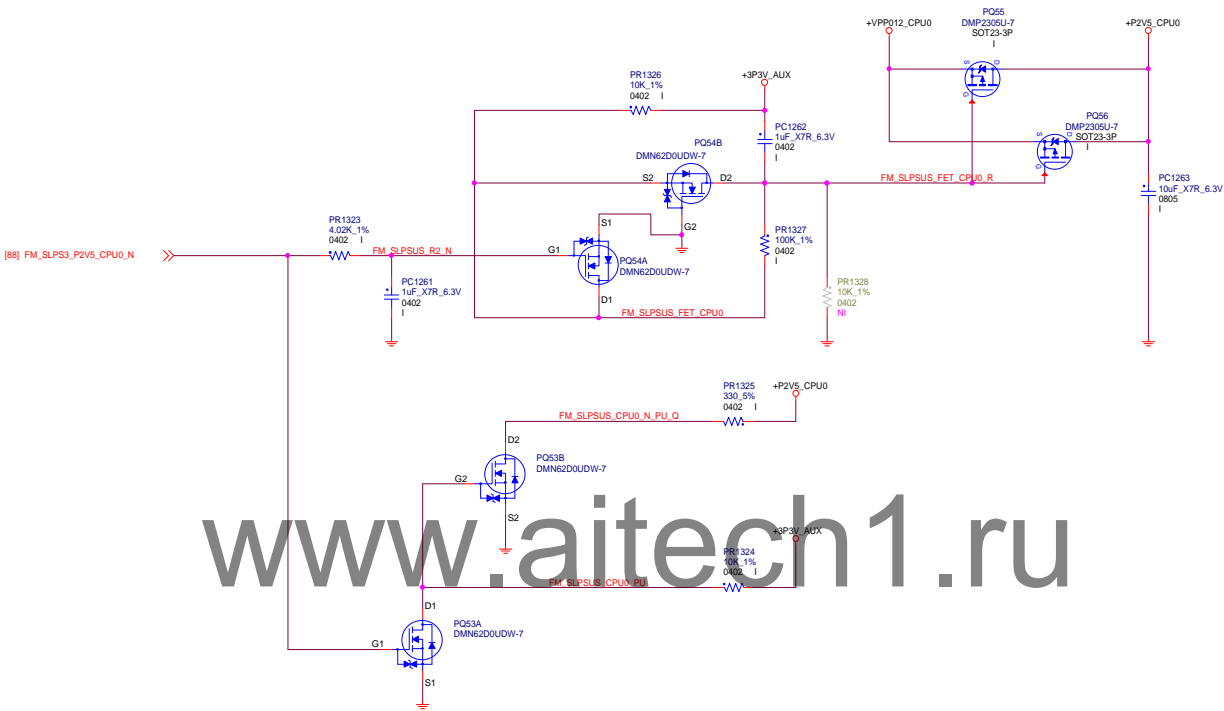
## +5V\_USBKB



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TITLE: VR\_5V\_STBY\_3.3\_AUX  
DWG NO.: MATIRA 5  
DATE: Thursday, June 29, 2017  
REV: A00  
SHEET: 143 of 150  
COMPRESSION IMAGE

+P2V5\_CPU0



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X01 to B02 modify list

20160901 EE

P079,P087: Add PCH TCM DISABLE\_N net name,add RS385  
P079,P104: Add POWERSHARE\_EN\_N net name  
P098: Remove USB3.0 Re-driver,add RU708  
P107: Add TCM  
P079,P107: Add PCH TPM DET net name  
P078: Add RF469,CF34,CK 24M 66M TCM  
P105 : Modify PWM Fan Controller from 2303 to 2305  
P106 : Modify FAN\_CPU0 to support LC FAN

20160902 DC

P129 :Change PC2142,pc2175 to 470nF from 680nF  
P131 :Change PC2147,pc2148 to 470nF from 680nF

20160906 DC

P139 :chang to reference PR2360 from PR2358  
P116 :Add PR2358,PR2359  
P104: Change net POWERSHARE\_EN\_N to PIN18

20160908 EE

P076 :Change RS5 to 10K ohm from 0ohm  
P084 :Populate RS112, RS115, Depop RS111, RS114  
P085 :Add RST\_I2C\_PCA9546\_N  
P103 :Del RST\_I2C\_1B/E\_PCA9546\_N and add RST\_I2C\_PCA9546\_N  
P110 :Del RO269

20160912 EE

Change silkscreen for DELL require

20160913 EE

P088:Move PWRGD\_CPU0\_DEF\_DRAM\_GTL from CPLD.K12 to CPLD.G15 for DELL require  
P076:Change RS5 form 10K to 12K for DC require  
P110:Update PCB information

20160913 DC

P142:PR2179 unstuff, ADD PR2401E-PR2402E-PR2403,PC2201  
P143:Change PR2360 to 100 ohm from 1Kohm  
P141:Add PD34

20160914 EE

P085,P087,P088,P105,P106:Change Fan control signal for DELL require

20160914 DC

P129:PC2142,PC2175 link datebase part  
P131:PC2147,PC2148 link datebase part

20160916 EE

Change title block for DELL require

20160920 EE

P041E-P087: Change RSR\_ERR\_N net to PWRGD\_CPU1\_GTL.. Connect to CPLD.M10 on M5 MB and CPU1.BC24 on M5 MEZZ.  
P108: Add RF478 to connect SPKR\_EN\_P1 and SPKR\_EN\_P2 and set BOM population option to "MP"  
P108: Add option to supply QA2 with +5V\_AUX  
P069: Convert SIO2 to black PCIe connector instead of blue  
P069,P070: Depopulate PCIe retention clips  
P108:Change Flexo-speaker circuit to follow Kepo example schematic. BJT should be on the GND side of the speaker and also include a diode  
P108,P088-P092:Connect PCH\_SPKR to CPLD.C5. Depopulate CA105, RA14, QA1.  
P104,P088,P085:Separate PCH\_PWRBTN\_N into two signals.  
1 - PWRBTN\_N connected to SW\_POWER1, PWR\_REMOTE, RF39, APS1.11, FRONTPANEL.8 and CPLD.D10  
2 - PCH\_PWRBTN\_N connected to PCH.M11, CPLD.T9 and dummy RO29  
P108: Add CRL for BUZZER

20160921 EE

P108: Change BUZZER schematic follow Matira7  
P092: Remove CA105,CPLD\_SPEAKER  
P085: Move PCH\_SLP\_S3\_N from EC\_F8 to EC.C11.  
P085: Disconnect PWRBTN signal from EC.D5. Instead change RO29 to 100K PU to V\_3V\_VBAT\_EC like other VCI\_nINx pins.  
P108: Cancel the PWRBTN change  
P107:Modify TPM co-lay SPI and LPC bus

20160922 EE

P085: Delete PWM&TACH for HDD\_FAN  
P110: Change PCB information

20160923 EE

P107: Add CHINA\_TPM\_EN and change BOM option  
P107: Add RF489  
P108: Change CRI CIS LINK and change reference to PA1

20160926 EE

P093: Change reference form AUD\_BPA&B to AUDIO\_A&B  
P084: Change values of RS111, RS110, RS114, RS79, RS80 to 1K to match PD value  
P107: Change "TCM" notes in schematics to "China TPM"

20160927 EE

P105:Add EMC1043 device on M5 MB, Use the SMBUS shared with the VCORE VR. Place EMC1043 DPI sensor on DIMM1 side of CPU.

20160928 EE

P105:Change Q046,Q047 package size from SOT23 to SOT1123

X02 to X03 modify list

20161012 EE

P092 :pop RA29,depop RA30 for Vendor request  
P025 :remove CPU0\_PC for Dell require

20161014 EE

P089 :pop RJ3

20161017 EE

P085 :Depop RO434/RO482/RO483

20161019 EE

P076 :Change CS1/2 value form 18pF to 15pF  
P084 :Del FW\_CMOS\_SERVICE;add PSWD,CMOS\_CLR,SERVICE\_MODE  
P084 :Add AIR\_Shroud Detection Switch  
P079 :Add GPP\_J2,GPP\_J3

20161020 DC

P141 :Change PR714 from 33 ohm to 10Kohm  
P104 :Change POWER\_CTRL Pin13 from +3P3V\_AUX to +3P3V

20161026 EE

P085 :Update UO\_EC CIS lick  
P105 :Update Q046&Q047 CIS link  
P041 :Add UPI\_PC for protect UPI connector

20161027 EE

P084 :Update PSWD,CMOS\_CLR,SERVICE\_MODE CIS link form PTH to SMD

20161027 DC

P128E\*PR2215 change from 294K to 267k 1%  
PR2240 change from 39k to 24k 1%  
P129E\*add 100nF PC2202 parallel to PC2142  
add 100nF PC2203 parallel to PC2175  
P130E\*PR2258 change from 294K to 267k 1%  
PR2281 change from 39k to 24k 1%  
PR2268 change from 71.5k to 44.2k 1%  
P131E\*add 100nF PC2204 parallel to PC2147  
add 100nF PC2205 parallel to PC2148

20161029 EE

P071,P072 :Pop RK9&RK30 for PCI LAN wake

20161031 DC

P142.:change PR2160 From 7.5K to 5.1K  
change PR2161 from 7.5K to 5.1K

20161104 DC

P144: Change PQ53,PQ54,PQ78,PQ79 from DMN65D8LDW-7 to DMN62D0UDW-7

20161104 EE

Change DMN65D8LDW-7 to DMN62D0UDW-7

20161107 EE

P109 :Change RH463 form 10K to 150ohm

20161108 EE

P106 :Change CPU fan design is 7pin for EE design and use 5pin connector

20161108 DC

P143:Change PQ31 to AON7407 from SISS27DN-T1-GE3

20161110 DC

P136:DUMY PR237E-PR220

20161111 EE

P106 :Change CPU fan colay design  
P076 :Change CS3/CS4 from 15pF to 8.2 pF of Vender suggest  
P085 :Change CO24/CO25 from 10pF to 18 pF of Vender suggest  
P085,P105 :Add HDD5 thermal diode signal for thermal team suggest

20161115 EE

P85 Del C0133  
P105 change HDD\_TEMP footprint

20161116 EE

P84 Del AIR\_SHROUD

20161117 EE

Update PCH information  
P106 :Add 12V to 3P3V level shift for LC\_FAN

20161122 EE

P105 :Change HDD\_TEMP silkscreen to THERM\_HDD  
P092,093 :Depop RA27,RA29,QA4,Pop RA30 and add RA66 for DELL require  
P075 :Change FLEX0 to FLEX0\_P0 and FLEX1 to FLEX0\_P1  
P089 :Change QL6 to SI4835DDY-T1-GE3 Follow M7

20161123 EE

P094,P095,P097,P099 :Change U08,U055,U056,U060,U061,U067,U069 EN PIN power form +3P3V\_AUX to +5V\_USBK8  
P084 :Depop RS112 and pop RS111

20161122 DC

P141:change PR718 from 86.6K to 169K  
chang PR713 fome 169K to243K

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DWG NO.	MATIRA 5	REV.	A00	
DATE	Thursday, June 29, 2017	SHEET	149 of 150	

